# DESIGN OF MULTI-BIT MULTI-PHASE VCO-BASED ADC

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## Abstract

*A design of multi-bit multi-phase VCO based ADC is presented in this paper. Time-domain quantization is done to extract the benefit from continuous scale down of technology Three stage current starved ring VCO is implemented using single ended delay cell configuration. A different method is used to increase the linearity of VCO and to increase the resolution of ADC in feed forward architecture, multi-bit quantization is done.*

***Keywords:*** *Multibitquantizer, noise shaping, oversampling delta–sigma A–D converter, voltage-controlled oscillator.*

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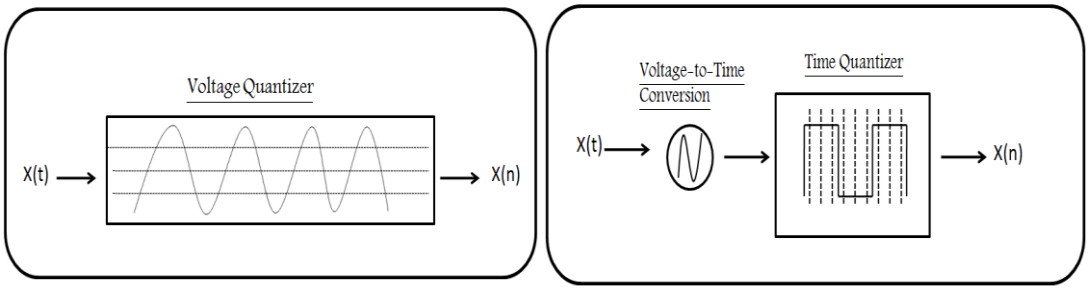
## 1. INTRODUCTION

Conventional ADCs (analog-to-digital converters) are built using analog circuits that quantize the input signal in the voltage domain. With scaling of technology, voltage dynamic range decreases as a result complexity of designing analog circuit increases [1]. Alternatively, time resolution improves with scaling of technology. VCO (voltage controlled oscillator)-based quantizers are highly digital circuits which quantize in the time domain instead of voltage domain, and hence, they are becoming more attractive in deeply scaled technologies. The VCO converts an analog voltage into time domain that can then be quantized using digital circuits [1] [2].

In earlier work, one-bit quantization is done on every delay element in ring VCO. Limiting feature of this design is that the maximum frequency of VCO should not surpass sampling frequency [3]. This limits the resolution of ADC to 3-4 bits in feed-forward architecture. In this work, to increase the resolution of ADC in feed forward architecture, multi-bit quantization is done. Also the non-linearity in tuning curve of severely degrades the performance of VCO-based ADC. This is because VCO no longer maps the input voltage to output phase in a linear manner. In present work a different method is used to increase the linearity of VCO [1].




1(a) 1(b)

**Fig 1**(a) Voltage quantizer, 1(b) Time quantizer

## 2. OVERALL ARCHITECTURE

VCO-based ADC consists of a 3-stage VCO to convert analog signal to an intermediate signals having frequency dependent upon analog input signal. Multi-bit quantized differentiator is used further to quantize the analog signal. A counter is then employed to count the edges. These edges are proportional to analog input value. A digital filter and decimator is then required to down sample the output of full-adder. A mapping circuit then can be used to map the different count of edges to corresponding digital bits.

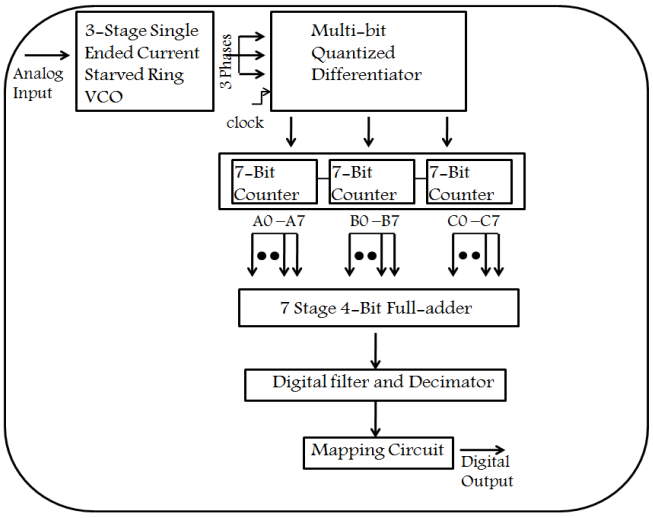



Fig **2** Implemented overall architecture

## 2.1 Ringvoltage-Controlled Oscillator

Three stage current starved ring VCO is implemented using single ended delay cell configuration. The linearity of ring VCO depends on the region of operation of current source (sink) transistors, and variations in $I_{BIAS}$ with $V_{TUNE}$. The nonlinearity of $I_{bias}$ can be reduced if NMOS transistor providing current bias is kept in saturation region until $V_{control}$ reaches $V_{DD}$. It increases the linearity of the oscillation frequency in the tuning range since$f_{osc}$ is proportional to $I_{bias}$. In addition to $I_{bias}$-$V_{control}$ characteristic, the operating region of current source(sink) transistors (CSTs) also determines the linearity of the VCO. When $V_{control}$ is low, the CSTs operate in saturation region and a wide range of frequencies are possible resulting in high $K_{VCO}$. When $V_{control}$ is high, CSTs operate in triode region and their gate voltages have less effect on $I_{bias}$

The design is implemented in UMC 0.18µm CMOS technology at 1.8V supply voltage. A wide tuning range of 66 MHz to 875MHz and having 94.5% tuning linearity is obtained.

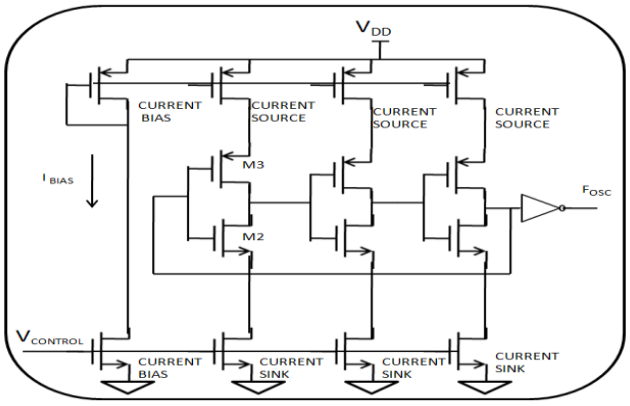



**Fig 3** Ring Voltage Controlled Oscillator

## 2.2 Differentiator

The block diagram of implemented differentiator is shown. Output phase is multi-bit quantized at both the rising and falling edges.

1) Multi-bit quantization: Since for one-bit quantization, maximum frequency of VCO should not be greater than sampling frequency, resolution of the ADC is constrained to 3-4 bits in feed forward architecture. To increase the resolution in feed forward architecture, multi-bit quantization is done.

The central aim here is to find out number of transitions a VCO element undergoes inside a given clock period by equating output of a particular VCO element for current and previous state with XOR function. The number transitions a VCO element undergoes inside a given clock period is dependent on delay generated by each VCO element. Delay generated by VCO element depends upon analog input voltage and indeed, resembles to the quantized value of analog input voltage.

Current and previous states of a particular VCO element are quantized using combination of two D-latches in series. Quantized values are further differenced with XOR gate.

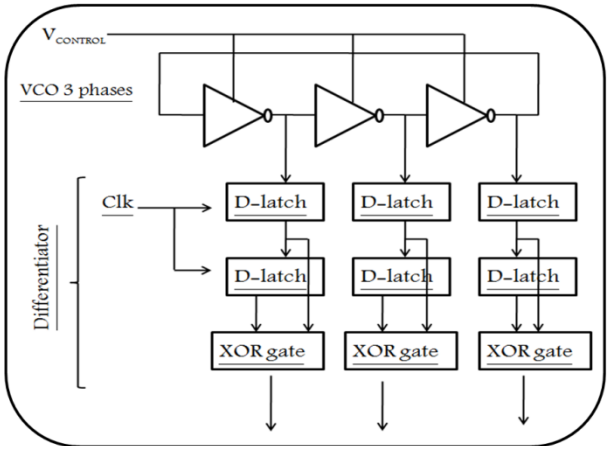



**Fig 3** Multi-bit quantized differentiator

## 2.3 Counters

Three 7-bit counters are then used to count the edges (and thus the frequency) that are generated by VCO for a particular input signal at each delay element. Three asynchronous 7-bit counters are designed using T-flip-flops, and the final count for each sampling period is stored in chain of D-flip-flops.

Output of the XOR gate is given as the clock to the first flip-flop. All succeeding flip-flops clock on the negative edge of the previous flip-flop's output. A reset signal is used to reset the counter after every 100 ns. The final count after every 100ns is stored in a chain of D-flip-flops.

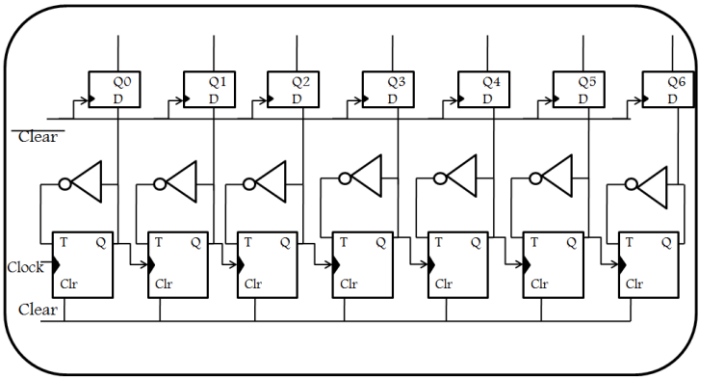



**Fig 4** 7-bit Counter architecture

## 2.4 Full-Adder

Next, a 7 bit full-adder is employed to add the count of all three counters after every 100ns.

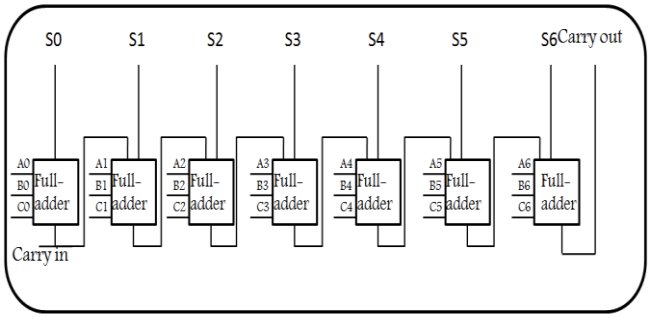



**Fig 5** Architecture of 7-bit full-adder

# 3. RESULTS

## 3.1 $V_{co}$ Frequency-$V_{tune}$ Characteristics

Parametric analysis is done to observe the variations in frequency with the tuning voltage. Tuning range is between 66 MHz to 875 MHz and linearity of 94.5% is obtained.

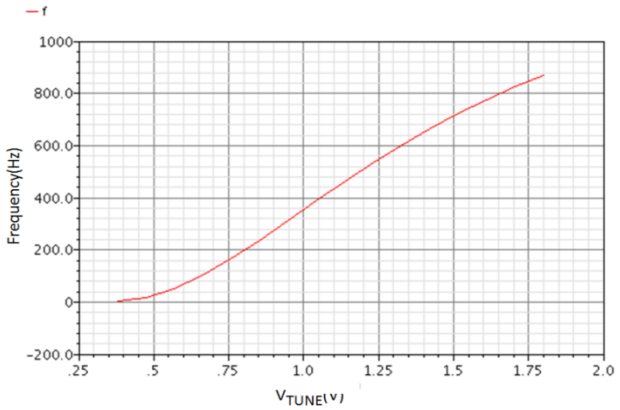



**Fig 1** Plot of frequency vs tuning voltage

## 3.2 Multi-Bit Quantized Differentiator Characteristics

Output from each delay element of VCO is quantized and differenced using combination of two D-latches and a XOR gate. D1 and D2 in figure 42 and 43 stores the current and previous state of a particular delay element for a particular instant of voltage, respectively. These two states are further differenced using a XOR gate. From comparing figure 42 and 43 it can be observed that the number transitions a VCO element undergoes inside a given clock period varies with analog input voltage.

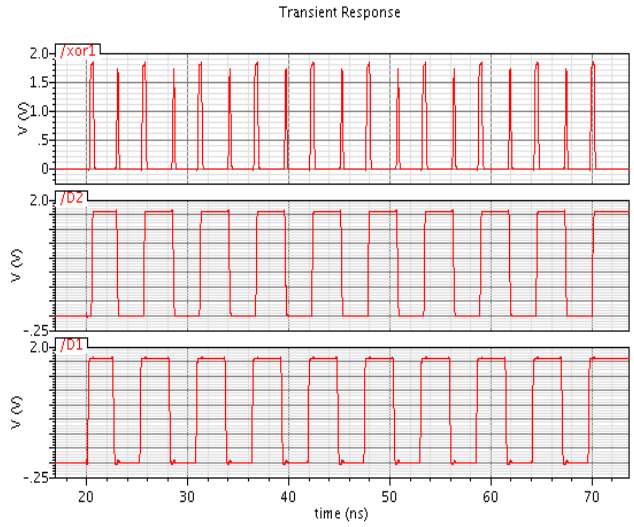



**Fig 2** Output multi-bit quantized differentiator for $V_{TUNE}$ = 800mV

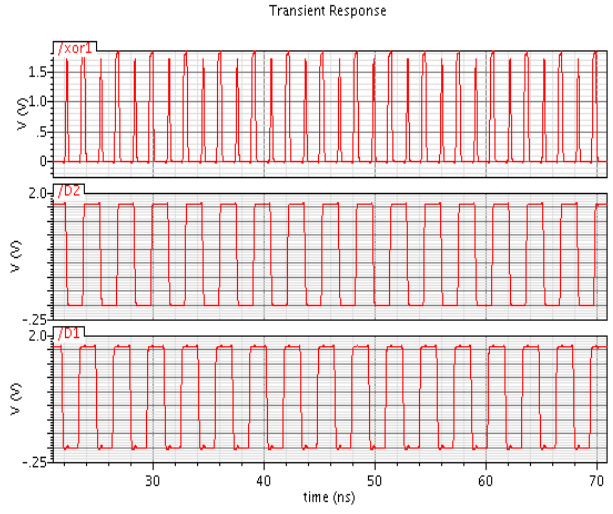



**Fig 3** Output multi-bit quantized differentiator for $V_{TUNE}$ = 1V

# 4. CONCLUSIONS

Voltage-controlled oscillator based analog-to-digital converter is a time-based architecture of which time resolution is improved by fast digital transition time from technology scaling. From the fact that, current quantization noise is correlated with previous quantization noise, first order noise shaping can be achieved inherently.

VCO-based ADC utilizing a three-element current-starved VCO core together with multi-bit quantized differentiator architecture is designed in this thesis. A different method is used to increase the linearity of VCO. A wide tuning range of 66 MHz to 875 MHz and having 94.5% tuning linearity is obtained from the VCO. This VCO performs the function of integrator in place of op-amp as in conventional delta-sigma ADC. Multi-bit quantization is used instead of one bit quantization to increase the resolution. Multi-bit quantized differentiator quantizes output phase of each element of ring VCO at both the rising and falling edges. Thus, the output phase of VCO is quantized by $\pi$ steps. Output of multi-bit quantized differentiator is further counted for each delay element of VCO, and the count is then added together using an adder circuit.

A quantizer of resolution of 7.6 bits is designed and first-order noise shaping is achieved. The resolution in feed-forward architecture is mainly limited due to inaccuracy of the differentiator.

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