AN APPLICATION SPECIFIC RECONFIGURABLE ARCHITECTURE FOR FAULT TESTING AND DIAGNOSIS: A SURVEY

A.R Kasetwar[1], Gaurav Kumar[2], S. M. Gulhane[3]

[1]Research Scholar,Dept. of Electronics & Tele communication, BDCE, Sewagram, Maharashtra, India
[2]P.G student Dept. of Electronics & Tele communication, DBNCOET,Yavatmal, Maharashtra,India
[3]Professor and Head of Dept. of Elect.& Telecomm.Engg, JDIET, Yavatmal, Maharashtra, India

Abstract

Now a day's many VLSI designers are implementing different applications on real time with the use of FPGAs. Although they are working efficiently, they are not achieving their expected goals. This is only because of the faults which are occurring in the FPGA at the runtime of the application. Those faults are remaining in the circuitry as there is no provision for removal of those faults at application level. So there is a great need of detection & removal of faults. Mainly Interconnect faults, Logical Faults and Delay are the faults which reduces the performance of FPGA. Although the manufacturers are trying to decrease the fault present in the FPGA, it is very necessary to remove those faults at run time of the particular application. This paper includes the brief discussion about the occurrence of different faults and various methods to remove those faults.

Key Words: *Fault diagnosis, field-programmable gate array (FPGA), testing.*

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1. INTRODUCTION

A Field Programmable Gate Array (FPGA) is a logic device that is used to implement a number of digital circuits. FPGA is widely used in many applications due to their reprogram ability, flexibility characteristic. It has also the advantage of short design & implementation cycles with low non-recurring engineering cost. As compare to Application specific integrated circuits (ASIC) FPGA results in faster design and debug cycle due to its reprogram ability. Though the density capability and speed of FPGA is increased, it becomes more vulnerable to various types of faults, but the FPGA test can be substantially more complex than application –Specific integrated circuit test. The basic architecture of FPGA consists of three major components: programmable logic blocks which implements the logic functions, programmable routing (interconnects) to implement these functions and IO blocks to make off-chip connections. We can Program FPGA for combination and sequential functions. All Programmable logic blocks (PLB) are Identical before programming. An illustration of typical FPGA architecture is shown in figure

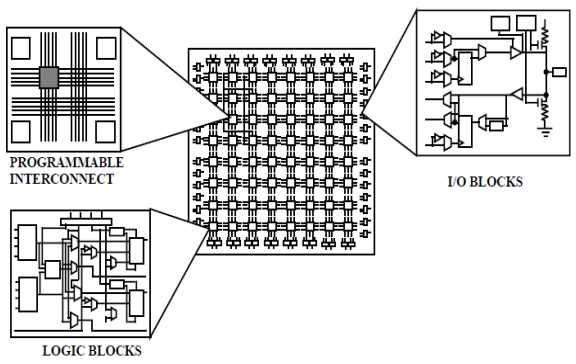

FIG.1 Basic Architecture of FPGA

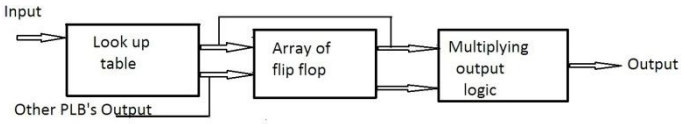

FIG.2 Typical Plb Structure

Above diagram shows the typical structure of programmable logic blocks (PLB) ; it consist of a memory block that can function as look – up table(LUT) or RAM, number of flip-flop(FFs); and multiplying output logic. The LUT/RAM block may also contain special-purpose logic for arithmetic functions (counters, adders, multipliers, etc.). The RAM may be configured in various modes of operation like synchronous, asynchronous, single-port, dual-port, etc. The FFs can also be configured as latches, and may have programmable clock-enable, preset/clear, and data selector functions [2].

The manufacturer of FPGA is constantly trying to decrease the number of faults, which are present in their designed FPGA. Detection of faults and the type of faults, which is present in the circuit, is known as fault detection. Fault diagnosis, process locate the fault in the circuit and replace or remove the faulty circuit with a good one.

In general, FPGA testing is of two types

1) Application Independent.
2) Application dependent.

Application independent tests are performed at the manufacturer level. In this test, entire FPGA resources are tested for the presence of faults. The faults usually focused

in this testing are logical faults and interconnection faults [21].

Compared to application- independent test and diagnosis, application –dependent test and diagnosis is faster with higher diagnosis resolution over more compressive faults [12].This is because application –dependent test focuses only on a specific part of FPGA used for a particular design instead of diagnoses complete FPGA. The faults of interest in this type of testing are only those that can affect the operation of a specific part of FPGA. It includes diagnosis of faults related to logic blocks, interconnection & delay faults which can strongly affect the timing characteristics of the circuitry. In this paper, we are focusing on the detailed study of various application dependent fault diagnosis methods. An application dependent fault diagnosis includes faults in the Logical blocks, Interconnect faults and fault due to the presence of delay.

Faults in the logic blocks are those faults which are related to Look-Up-Table (LUT), multiplexers and with the flip-flops. For an LUT, a fault can occur in any of the memory matrix, decoder, and input output lines. A faulty memory matrix makes some memory cells incapable of storing the correct logic values. If the fault is related with the decoder, then a wrong address may lead to reading of wrong cell contents. The next possible fault is related to input output lines that led to generation of the stack at fault. The multiplexer faults are functional faults because the internal connection of multiplexers in FPGAs is different for different application. Faulty multiplexer may have the problem in selecting correct inputs applied to it. The faults in flip-flop are also a functional fault any fault can cause a flip-flop to receive no data, to be unable to be triggered by the correct clock edge, or to be unable to be set or reset.

The interconnect faults are the faults which are generated due to the fault in connecting wires [22]. It may be an open fault, short fault or stack-at-faults. The other type of fault is a delay fault which may severely affect the timing characteristics of the output. It is an important task to test whether an operation is completed within the specified clock cycle or not. Though a circuit is free from logical and interconnection fault, the output characteristics may get badly affected.

2 PREVIOUS WORK

2.1 LOGICAL FAULTS

TomooInque et.al proposed a universal fault diagnosis method for unprogrammed FPGAs, based on a test procedure for Configurable logic blocks (CLBs) developed by Michinishi. Author's method is used to diagnose one CLB i.e. method is used to locate the fault in only on CLB. Their assumption is that there is at least one CLB which includes faults like Stuck-at, interconnect, multiple-access faults of look-up-table. They had performed their procedure repeatedly by implementing a configuration and alternately applying input sequence to the configuration. TP_{CLB} is represented by a sequence of pairs consisting of a configuration and input sequence applied to the configuration as follows:

$TP_{CLB}= [(C_1, S_1), (C_2, S_2)....., (C_{2k+1}, S_{2k+1})]$
This test procedure detects any faults in faulty block. However this method requires repetitive computations, which lead to consume much time for testing.

A hybrid fault model for FPGA testing was introduced in 2001, which permits the detection of all single faults (i.e. stuck –at faults, functional) with some multiple faults [2]. Repeated FPGA reprogramming is used. They had assumed that interconnects and IOB's had already tested. The main objectives of their proposed method is

a) 100% fault coverage with neither delay nor area overhead.
b) Ease of test pattern generation because test patterns generated for CLBs, not for complete FPGA.
c) Efficient implementation of the testing process.
d) Number of programming phase must be as small as possible.

Author had generated test pattern into two phases according to the CLB partitioning. The LUT memory matrix can be tested by reading all the memory bits in two phases; second phase is complement of the first. For testing stuck-at faults, the scenario is different. The contents of LUT must be arranged such that Boolean difference is one for input to be tested for which multiple patterns are required. For multiplexers, each data inputs must be activated at least for one phase because multiplexers selects single output from all inputs i.e., at least $n_i$phases are required to test a multiplexers with $n_i$input. Advantage of using this method is that the time required to test all the CLBs is the same as to test a single CLB with perfect controllability/observability. All the CLBs can be under test simultaneously, which is not possible with other method like neither BIST approach nor naive approach.

Faults related to CLBs are solved correctly in the method proposed [2], but the problem of testing faulty multiplexers was solved incorrectly. A new built-in-self –test approach which is able to detect and accurately diagnose all single and practically all multiple faulty PLBs in FPGA with maximum diagnosis resolution was proposed by M.Abramovici and C.Stroud.[5]

The logic and interconnect faults are tested separately; it is an offline testing method. The problem related to conventional BIST approach is the problem area overhead and delay penalties; which later results in speed degradation, which is unacceptable in high performance system. The BIST methods are first proposed for testing PLBs and then extended for testing interconnects faults.

To configure groups of PLBs as Test Pattern Generators (TPG), Out Response Analyzer (ORA) and other group as Block Under Test(BLT) as shown in fig 3 (a). The BUT is reconfigured repeatedly to test it in all modes of operation. Once the BUT is tested, the role of PLBs is reversed so that

in the next test session the previous BUTs become TPG or ORAs and vice versa. Fig 3(b) & 3 (c) gives the floor plan for two test session. Authors had used Pseudo exhaustive testing method.

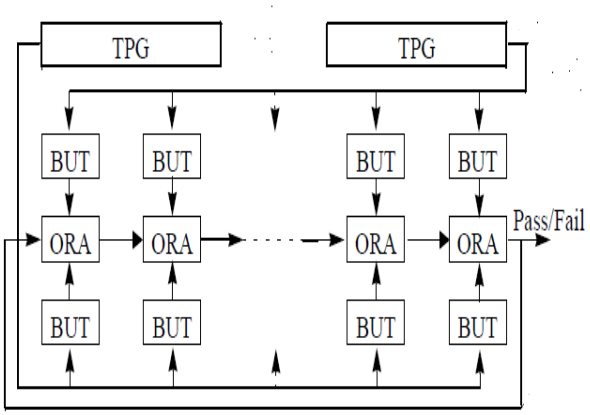

FIG.3. BIST Architecture TPG, BUT and ORA Connection.

	a)		b)
1	TPGs	1	BUTs
2	BUTs	2	ORAs
3	ORAs	3	BUTs
4	BUTs	4	ORAs
5	ORAs	5	BUTs
6	BUTs	6	ORAs
7	ORAs	7	BUTs
8	BUTs	8	TPGs

FIG.4. A) Floor Plan for First Test Session B) Floor Plan for Second Test Session.

Following claim had been made: Any single faulty PLB is guaranteed to be detected, with the group of faulty PLBs in the same row is guaranteed to be detected also group of faulty PLBs in the middle rows of the same column that has at least two adjacent faults free PLBs is guaranteed to be detected.

Most of the authors had focused on application independent diagnosis of FPGAs. Application dependent diagnosis of FPGAs techniques for logic and interconnect resources was introduced by M.B.Tahoori [17]. For logic diagnosis, the configurations of used logic blocks remain unchanged while the configurations of theInterconnect resources and unused logic blocks are modified. Any single functional fault, inclusive of all stuck-at faults, in logic blocks are accurately diagnosed in only one test configuration.

The problem with previous testing is that it diagnose only those blocks which are used in some particular application where as other blocks, which are not used for that operation may introduce new faults. This affects the reliability of the system. A new technique for online testing and diagnosis of nontransient faults in PLBs with the help of roving self-testing-area (STARs) is introduced [6]. The STAR is a temporarily off line section of the FPGA in which self-testing continues without affecting the actual operation of FPGA. BIST approach detects any combination faulty PLBs. During the testing process, BIST approach is used to test all PLBs in the BISTER tile. The main advantage of this testing is that if a particular fault is not obtained, the suspected faulty PLBs are divided into subset and retested. The diagnosis time is very fast.

Further J. Emert et.al had introduced new Fault Tolerating (FT) techniques for PLBs. In previous FT techniques, faults are detected within the working part of the system, and then they are located or bypassed as quickly as possible so that working of the FPGAs does not get affected. In STAR technique, the FPGA is divided into two parts. The STARs where the BIST and diagnosis take place and the working area where operation is carried out. When the test of one part is completed, STAR exchanges its part so that it can cover complete FPGA. The main advantage of this technique is that the fault is detected in an STAR due to which they do not affect the working of the system. This technique is used only for the logical faults. Authors had determined whether the system can continue it works under the presence of the located faults or not. Because in many situations this is possible due to which no reconfiguration is needed, but if fault affects the system function, alternative configurations was determined that avoid the faulty resources. This method allows more time for accurate diagnosis and for computing any required fault by passing configuration. This method determines the faulty LUTs or the faulty FFs inside a PLB.M.B.Tahoori had focused on logic and interconnect faults. For the logic faults, Built – in –self-Diagnosis (BISD) method is used in which the configuration of used blocks remain unchanged while the configuration of the interconnect resources and unused logic blocks are modified. In this method, any functional fault is accurately diagnosed. [11]

In this scheme, all used logic blocks were tested exhaustively. In which global interconnect is reprogrammed such that test signals are routed to each logic blocks. A Linear feedback shift register (LFSR) is used for generating test vectors, which are connected to all logic blocks. The output of logic blocks is connected to internal response compactor. The number of the test session in this technique required is less as compare to others. While in other cases, the time requirement is also more and even then those methods focus only on single faults.

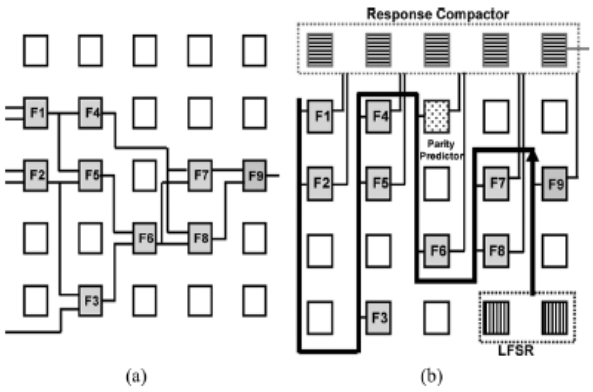

FIG.5 Application –Dependent Self-Test Architecture For Logic Blocks A) Original Configuration B) Bist Configuration.

2.2 INTERCONNECTION FAULTS

Detection of interconnection faults in FPGAs circuit is a difficult problem. In year 2002, M.B.Tahoori proposed a new method to diagnosis open defects present in the circuit. An open defect is a discontinuity in the connection between two circuit's nodes that should be completely connected [13]. Author had proposed a two-step diagnosis processes to identify the faulty interconnects blocks. In which the first step is Coarse –grain step which localizes the fault to a small portion of the FPGA. In the second step i.e. fine grain step, it precisely locates the faults inside that portion of the FPGA.

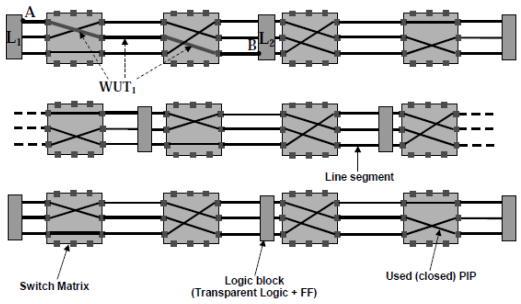

FIG.6. A Test Configuration For Interconnect

In the above figure test configuration consist of the number of wires under test (WUT). A WUT consist of the routing paths which connect the output of one logic blocks with the input of other logic blocks. During the diagnosis process, the logic value of WUT is captured, and the values are stored in the flip- flop connected to it in the next cycle. The value stored in the flip- flop is verified by applying it to the test vector, and the faulty WUT is obtained. Input to the fine grain diagnosis is a defective WUT, which is the output ofCoarse –grain. In this step, the goal is to identify faulty recourses. The basic idea, which is used here, is a portion of WUT is removed and using some other WUT connection is made. If the new WUT still fails which means those removed WUT are faults free, i.e., the fault is located in the non-removed recourses. Otherwise, the opposite conclusion is made. The time required for diagnosis of interconnect is large because the complete process is performed in two parts and 100% fault removal is also not guaranteed.

Further G.Hriss et.al had suggested a new method to diagnose faults in Cluster based FPGAs [14]. The fault detection in cluster based FPGAs are very difficult because of its high densities. Author had used BIST method they had focused on two possible faults present in the FPGAs an open fault in which a single line is broken, or a connectable cable is unconnected and short defect which causes two lines to be crossed. However, the diagnostic resolution was limited to a given set of WUT, and far from the diagnostic resolution required for efficient fault tolerant application.

According to M.B.Tahoori interconnects diagnosis for the configurations of used logic blocks are modified and interconnect configuration remain unchanged [11]. Any single fault (open, stuck-at, or bridging fault) in interconnect can be uniquely identified in a small number of test configurations. Author had categorized the diagnosis procedure into two parts (a) Adaptive (b) Non adaptive approach. In adaptive approach, the selection of the next step is depending on the result of the previous step. Whereas in non-adaptive process all the steps are performed first and then the result is calculated from falling pattern. The non-adaptive approach is preferred over adaptive approach because the time requirement is less

2.3. DELAY FAULT

Delay fault diagnosis is more difficult as compared to interconnect faults as delay fault model depends on the size of a delay defect due to which it is harder to define. Path delay testing of FPGAs is very important because FPGAs which is fault free will, still not work properly due to delay. The basic idea is to test a set of interconnects, or paths, between two logic blocks for delay faults by creating a race condition between the signals propagating on those paths. The particular set of paths under test (PUTs) between two logic blocks are configured such that their fault-free propagation delays are nearly identical, and a signal transition simultaneously occurring at the start of the PUTs should also simultaneously occur the end of the PUTs. [15]
In the above method, an iterative logic array model is used which test number of similar sections of interconnects simultaneously [16]. Author had suggested a new approach which partitions target paths into subset which are used in the same test configuration. They had tested all the paths with all combinations of signal inversions. As there are numbers of paths present in the circuit only a limited sets of the path is tested, with the guarantee that the maximum delays along the tested path will not exceeds the clock period during the normal operation. They had proposed two methods in the first method, which is known as single – phase method; paths are selected so that all paths in each configuration can be tested in parallel. Whereas the second method is the multi-phase method; attempts to test the paths in a configuration with a sequence of test phases, each of which test a set of paths in parallel.

All the previous authors had delayed fault testing for general integrated circuit. Nur A.Touba et.al had proposed a new method to delay diagnose [26]. The method is simple and

easy to apply. CLBs are reprogrammed, and then the modified circuit is tested by using the same test pattern which caused the circuit to fail. As the same test pattern is re-used, it eliminates the time that is required for generating additional diagnostic vectors. This technique targeted towards the common case of single point delay defect that increases the delay through a CLB or an interconnect causing it to exceed its timing specification.

3. SUMMARY AND CONCLUSION

Fault diagnosis has particular importance in the context of field programmable gate arrays (FPGAs) because faults can be avoided by reconfiguration at almost no real cost. The main faults in the FPGAs are interconnects, logic blocks and faults related to delay of an arbitrary design. As FPGAs works properly, all three faults should be removed. FPGA testing is of two types an application dependent and application independent. The testing process for both is different. The time required to test an application dependent testing is less as it focuses only on some specific part whereas the application independent testing tests complete FPGAs.Faults related to logical block, interconnected faults and delay faults are the problems for the FPGAs user. Numbers of faults diagnosis method are present.

In this paper, we have made a detail survey of number of methods for fault diagnosis from this survey we come to know that for interconnect diagnosis, the method explained by M.B.Tahorri [11] is better as compared to other method because all the single faults and multiple faults (open, stuck-at –faults, or bridging faults) are uniquely identified and removed. For logic blocks diagnosis, BISD approach is selected because in it multiple faults are uniquely identified in a single test configuration with a fixed test time. All other methods are limited only for faulty CLBs and single faults [11].For delay fault the method proposed by JayabrataGhosh is preferred. It is used for both manufacturing as well as user configuration test with the guarantee that the maximum delays along the tested path will not exceeds the clock period during the normal operation.

TABLE- 1: Comparison of Different Methods

Reference	Logic Blocks	Interconnection	Delay faults	Conclusion
[1]	Yes	NO	No	Only one fault considered
[2]	Yes	NO	No	Only one fault considered
[5]	Yes	NO	No	Two test session for all CLBs
[6]	Yes	NO	No	Accurate only for single faulty PLB and for some multiple PLBs
[9]	Yes	NO	No	Used for online operation
[11]	Yes	Yes	No	For logic block only one test configuration and for interconnect it logarithmic depends on the FPGAs size
[25]	No	No	Yes	Used by Manufacturer
[26]	No	No	Yes	Time required is small & used by manufacturer and user

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BIOGRAPHIES

A.R. Kasetwar is a research scholar from BapuroDeshmukh College of Engineering, Wardha working in the field of D.S.P-VLSI (phone: 9766813382; E-mail: abhaykasetwar@gmail.com).

Gaurav Kumar is pursuing his M.E from Dr.BhausahebNandurkar College of Engineering and Technology, Yavatmal India (phone: 9860402620; E-mail:singhgauravsep@gmail.com)

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Dr.S. M. Gulhane working as a Professor and Head of Dept. of Elect. & Telecomm. Engg. and holding a charge of Dean (Admin.) at Jawaharlal Darda Inst. Of Engg. & Tech., Yavatmal,(phone 9881832100; E-mail : smgulhane67@rediffmail.com)