MULTIPLE GATE FIELD-EFFECT TRANSISTORS FOR FUTURE CMOS TECHNOLOGIES

Suhas N.Yadav[1], M.S.Jadhav[2]

[1]*Department of E & TC Engineering,Dr.JJMCOE, Jaysingpur*
[2]*Department of E & TC Engineering,.AIT (Polytechnic), Vita.*

Abstract

This is a review paper on the topic of multiple gate field effect transistors: MuGFETs, or FinFETs, as they are called. First, the motivation behind multiple gate FETs is presented. This is followed by looking at the evolution of FinFET technologies; the main flavors (variants) of Multigate FETs; and their advantages/disadvantages. The physics and technology of these devices is briefly discussed. Results are then presented which show the performance figures of merit of FinFETs, and their strengths and weaknesses. Finally, a perspective on the future of the FinFET technology is presented.

Keywords*: CMOS scaling, Double gate MOSFET, FinFET, Multiple gate FET, Multigate FET*

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1.INTRODUCTION

In this paper, we have taken a comprehensive look at undoped double gate MOSFETs, also known as MuGFETs or FinFETs, which are promising candidates for scaling CMOS into the sub-32 nm era on account of their potentially improved channel control and reduced dopant fluctuations. We first presented the motivation behind multigate FETs, and then traced the evolution of multigate FETs, and also discussed the classification of multigate FETs based on current flow. We then outlined the aspects of the FinFET's fabrication technology. We then went into the many aspects of the FinFET's performance by looking at their DC, low-frequency analog, and high-frequency (RF) performance parameters, and by benchmarking the FinFET's performance with that of the planar bulk MOSFET, and discussing their relative merits and demerits. No discussion on FinFETs would be complete without discussing the impact of the fin width. Here again, we looked at the many trade-offs involving fin width considerations. We also discussed briefly the noise and mismatch performance of FinFETs and concluded by making an overall assessment of the FinFET technology.

1.1.Motivation Behind Multigate Field-Effect Transistors:

The phenomenon of short channel effects (SCEs) in metal-oxide-semiconductor field-effect transistors (MOSFETs) has been known since the late 1970s. As gate lengths are reduced, threshold voltages are seen to decrease and OFF-state currents are seen to increase. This is a consequence of the fact that as gate lengths are decreased, the depletion regions associated with the source-to-body and drain-to-body regions become closer to each other and start to interact with each other. Since depletion regions are regions of high electric fields, they facilitate carrier transport directly between the source and drain regions, which gives rise to the observed phenomena of higher OFF-state currents, reduced threshold voltages, and reduced control of the gate over transistor characteristics in MOSFETs. Classical scaling approaches have dealt with this problem by requiring an increase in body doping, thereby decreasing the depletion widths associated with the source-to-body and drain-to-body regions, so that these two junctions are kept separated to the extent possible. However, increasing the body doping is accompanied by severe drawbacks such as degraded mobilities, increased capacitances, and increased statistical fluctuations, all of which pose serious challenges to scaling. Innovative solutions such as dynamic threshold voltage MOSFETs (DTMOS) have been successfully used to reduce the leakage power consumption of analog and digital circuits.

An alternate way to increase the gate control over the channel would be to have an extra gate. This additional gate would help strengthen the immunity of the channel from penetration effects of the drain electric field. In this approach, the main lever for controlling the channel is not with the body doping, but the separation between the two gates. In fact the body doping is deliberately kept at a very low value, at near-intrinsic levels. This helps avoid the problems of mobility degradation, higher junction capacitances, and stochastic fluctuations. Undoped double gate MOSFETs (DG MOSFETs) are thus a better option from the point of view of long-term scalability and extend ability to future CMOS technologies.

2. EVOLUTION OF MULTIGATE FETS

The seriousness of the problem of short channel effects in single gate MOSFET transistors, and the potential difficulties associated with their scaling by increasing body doping became evident way back in the early 1990s, and many true DG MOSFET architectures were proposed. A very good overview of these architectures is given in based

on their orientation, Wong grouped the double gate architectures into planar (or Type I), vertical pillar (or Type II), and vertical (or Type III). These are illustrated in [Figure 1].

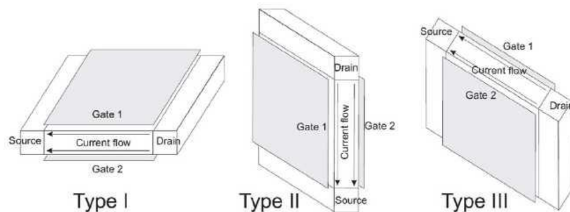

Fig-1: Double gate MOSFET Topologies

In 1990, Hisamoto proposed a Type III DG MOSFET topology with the name fully depleted lean-channel transistor (DELTA). The DELTA topology did not gain momentum at that time since the classical planar MOSFET topology was meeting the transistor specifications satisfactorily.

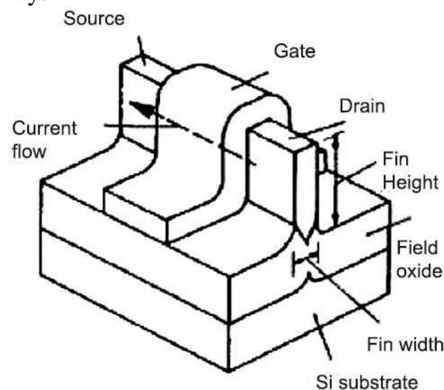

Fig-2:he Fully Depleted Lean Channel Transistor (DELTA) topology, introduced in 1989

In the subsequent years, as scaling challenges became more severe, the DG MOSFET architecture was revisited, and the DELTA topology made a comeback a decade later, this time under the name 'FinFET'. This time, it captured the attention and fascination of the scientific community, and the subsequent few years saw an explosion in research and development efforts into FinFETs

. There are two minor variants of the FinFET, namely, the omega-gate FinFET and the pi-gate FinFET, which are named following the shape of the overlapping gate over the fin. In the case of the omega-gate FinFET, the gate undercuts and partially covers the bottom surface of the fin as well, whereas in the case of the pi-gate FinFET, the gate extends to a depth below the bottom of the silicon fin. The objective of these structures is to achieve an additional gate control over the channel and prevent fringing fields from penetrating into the silicon body. [Figure 3] shows these two variants of the FinFET.

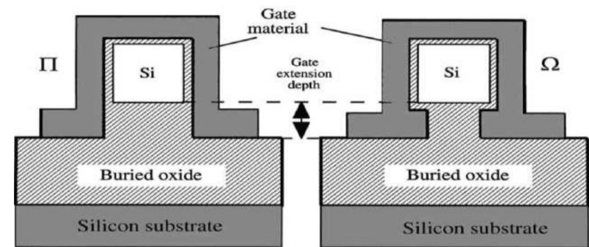

Fig 3: Pi- and Omega-gate FinFETs.

And then we have the gate wrap-around FET, or gate all-around (GAA) FET, or surround-gate FET, where the silicon is surrounded on all sides by the gate. Such a transistor is also known as a nanowire FET, and represents the ultimately scaled MOSFET device, i.e., the device with the maximum possible gate control over the channel. This device is shown in [Figure 4]. Such a device was proposed as early as 1990.

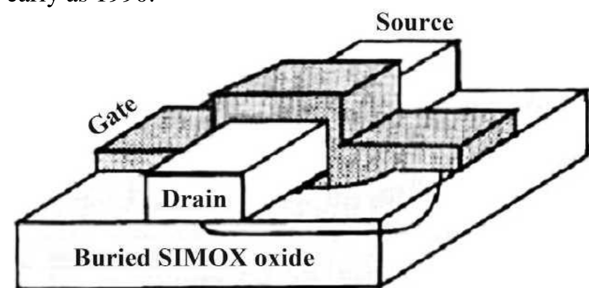

Fig-4: Gate wrap-arround or Gate all-round FET.

3. FABRICATION TECHNOLOGY

The FinFET process can either follow a "gate-first" route, or a "gate-last" route. In the former route, fin formation is followed by gate stack formation followed by extension formation, whereas in the latter route, fin formation is followed by extension formation followed by gate stack formation.

Both routes have been used for fabricating well-functioning FinFETs down to 20 nm gate lengths. FinFETs are fabricated with fin widths that are typically less than one-half of the minimum gate lengths.

Such dimensions are typically sublithographic, and not possible to define directly in a single-step process. Techniques such as e-beam lithography can be used to pattern the fins directly; however, this route is not preferred for production due to high equipment cost and low manufacturing throughput.

Hence fin patterning needs to make use of creative techniques in order to pattern such sublithographic dimensions. Two of the mainstream techniques for fin definition are resist-defined fin (RDF) patterning and spacer-defined fin (SDF) patterning. A schematic flow of the RDF process is shown in [Figure 5].

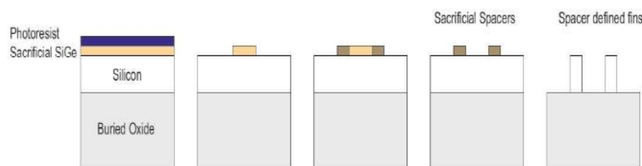

Fig-5: Process flow for Resist Defined Fin (RDF) technology.

In this process, a thick (≈ 100 nm) hardmask is deposited on the silicon. This is followed by a deposition of a positive photoresist and exposure using 193-nm DUV lithography in order to define the active areas. Unexposed areas of the photoresist are removed, exposing the hardmask beneath, which is then etched using an anisotropic etch process. After the hardmask is removed from the exposed areas using a HF-based isotropic (wet) etch, trimming of the resist/hardmask stack is performed in order to reduce the thickness down to the desired sublithographic dimension.

Once the hardmask thickness has been brought to the desired value, once again an aggressive, directional etch is carried out, this time etching into the silicon film, while the resist/hardmask combination serves to protect those areas that will eventually form the fins. This etch is continued till all the unprotected silicon has been etched away, and then the hardmask on top of the silicon is also removed to reveal the fin areas.

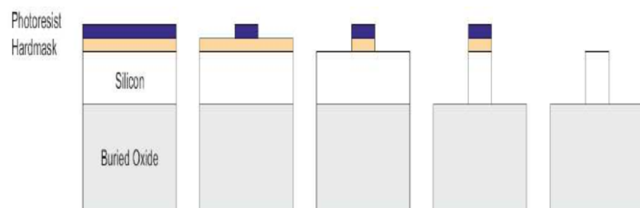

Fig-6: Process flow for spacer defined Fin Technology.

A schematic of the SDF process is illustrated in [Figure 6]. In this approach, a sacrificial SiGe film is blanket deposited on top of the silicon film and patterned in such a way that the width of this sacrificial SiGe defines the final fin-to-fin spacing. This is followed by the formation of a thin nitride spacer along the sidewalls of the SiGe. Next the SiGe is removed, leaving behind the nitride spacers, which serve as a hardmask during the subsequent etch of the silicon film. The thickness of the spacer translates into the resulting width of the fins. This is the SDF formation process. Depending on the process control and the desired fin widths, this process of sidewall spacer formation and etching can even be carried out one more time to result in even smaller fin widths. High fin patterning densities can be obtained using the SDF process; however, in this instance the fin width is fixed by the technology, and it is not possible to use it as a design variable, since arbitrary fin widths are not supported in this technology.

Fin width definition is followed by a hydrogen annealing step in order to relax the stresses and defects at the surface which may have resulted due to aggressive etch chemistries employed for fin definition. This hydrogen annealing step also smoothens the sharp edges of the FinFETs cross section, resulting in a rounded profile, which reduces the problems of electric field crowding and corner effects. [Figure 7] is a top view of a FinFET before and after hydrogen anneal, showing the effect of corner rounding.

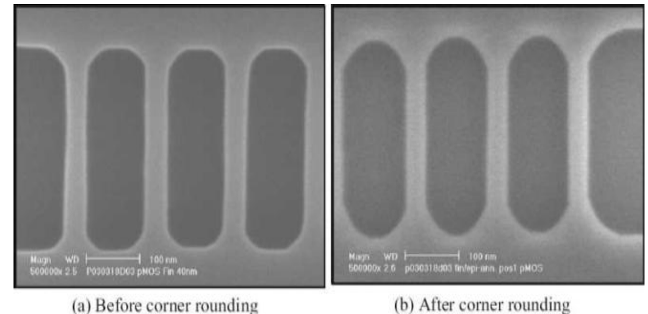

Fig-7: Top view of a FinFET before and after corner rounding step.

The fabrication sequence is shown schematically in [Figure 8].

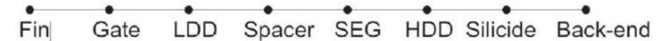

Figure 8: Main modules in the FinFET fabrication sequence. In the gate-last process the source/drain is formed immediately after fin patterning. Doped polysilicon or polycrystalline SiGe is deposited on the fin, followed by a patterning which defines the source/drain extension regions. Spacer is grown on the insides of this region, and is followed by gate stack deposition and patterning. A picture of the FinFET at the end of its fabrication sequence is shown in [Figure 9].

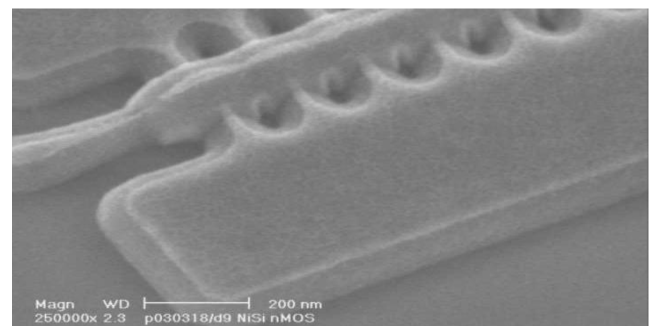

Fig-8: The FinFET at the end of the Front-End-Of-Line (FEOL) steps.

4. DEVICE PERFORMANCE

To assess the DC and low-frequency analog performance, we look at device parameters such as the parasitic resistance, mobility, saturation velocity, and corresponding figures of merit such as the drive current (I_{ON}), leakage current (I_{OFF}), transconductance (G_m), output conductance (G_{ds}), and voltage gain (G_m / G_{ds}). These are obtained from *I-V* and low-frequency *C-V* measurements. To assess the high-frequency (RF) performance, we perform two-port S-parameter measurements from which we obtain the high-frequency transconductance, output conductance, parasitic resistance, and capacitance, and corresponding RF figures of

merit such as the unity gain current frequency (or cutoff frequency), f_T , and the unity power gain frequency (or oscillation frequency), f_{max} . There are also important considerations such as low-frequency noise, high-frequency noise and current mismatch, and the overall device performance is thus a complex function of all of these. The FinFET's performance also depends strongly on the width of the patterned fins, known as the fin width. In this paper, we will show trends in some of the key device parameters and figures of merit for FinFETs, and compare them with those of planar bulk MOSFETs.

4.1 DC and Low-Frequency Analog Performance

4.1.1 Source/Drain Resistance

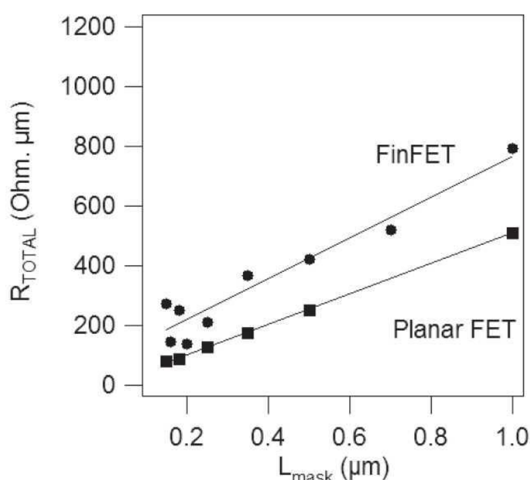

Fig-9: Source/Drain resistance extraction from a plot RTOTAL vs L.

The S/D Series resistance of FinFETs is seen to be 3-4 times higher than planar MOSFETs. This is due to higher spreading resistance encountered in FinFETs due to its 3-dimensional current flow path.

4.1.2 Mobility and Saturation Velocity

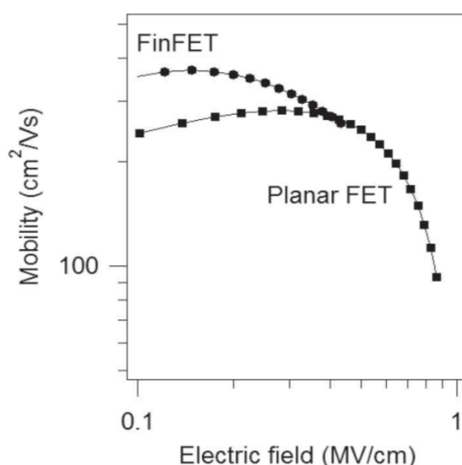

Fig-10: Comparison of mobility in FinFETs versus planar bulk MOSFETs.

At lower electric fields, mobility of FinFETs is higher owing to reduced coulomb scattering which is due to their lower doping. Mobility is extracted using the split CV method, and the channel length is equal to 1 Ām.

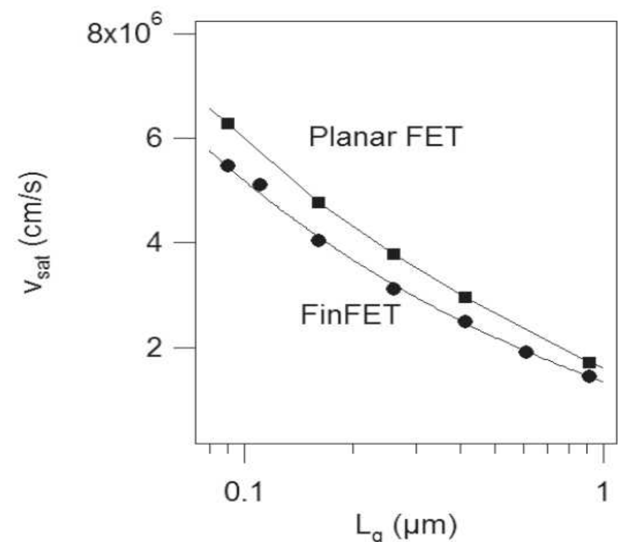

Fig-11: Comparison of saturation velocity in FinFETs versus Planar bulk MOSFETs.

Due to the dominant (110) orientation, and due to the smaller volume available for current flow, in FinFETs, their saturation velocity is lower compared to planar MOSFETs. Saturation velocity is calculated as the ratio of peak

4.1.3 Transconductance and Voltage Gain

Two of the important analog figures of merit are the transconductance (G_m) and the voltage gain (A_v).

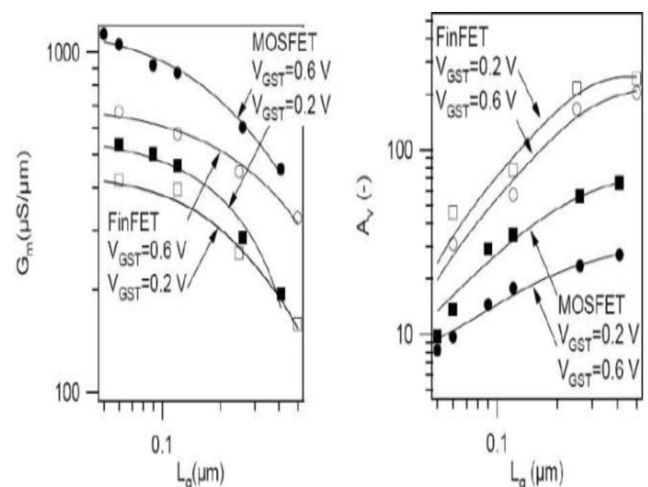

Fig-12: Length scaling of transconductance (Gm) and voltage gain (Av) of FinFETs and planar MOSFETs.

FinFETs show a lower transconductance on account of a higher series resistance and lower saturation velocity, and a

higher voltage gain due to a much lower output conductance which offsets the reduced transconductance.

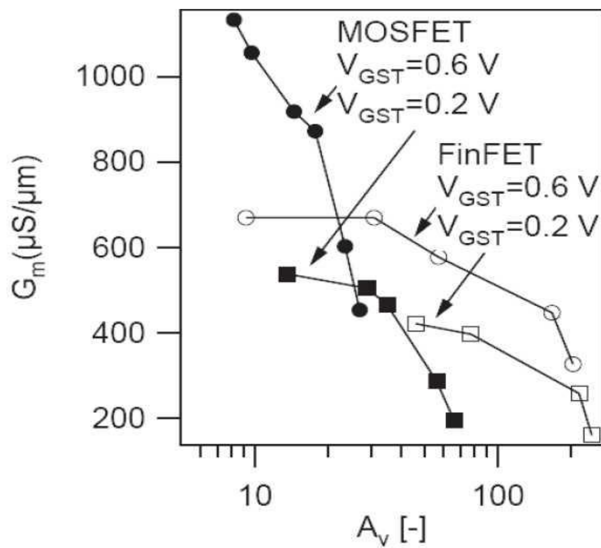

Fig-13: Plot of transconductance (Gm) versus voltage gain (Av) of FinFETs versus planar bulk

MOSFETs for gate voltage overdrives of 0.2 V and 0.6 V. Dark symbols represent planar bulk MOSFETs, while light symbols represent FinFETs. Planar bulk is able to reach high Gm but at reduced Av, while the opposite is true for FinFETs.

4.2 High-Frequency (RF) Performance

Till now we have looked at the DC and low-frequency analog performance of FinFETs and benchmarked it against that of planar FETs. FinFETs are observed to have a high source/drain series resistance, which degrades their currents and transconductances. At RF frequencies, the device performance is additionally impacted due to parasitic capacitances. There are several components of parasitic capacitance in a conventional planar MOSFET. These comprise the outer fringing capacitance (C_{of}), the inner fringing capacitance (C_{if}), the overlap capacitance (C_{ov}) and the top plate capacitance (C_{top}). These are shown in [Figure 15].

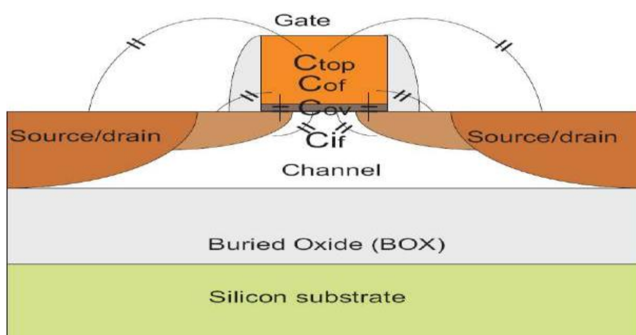

Fig-14: Parasitic capacitances in a conventional planar MOSFET.

It is comprised of the top fringing capacitance, outer fringing capacitance, inner fringing capacitance and the and gate overlap (or LDD under lap) capacitance. In a FinFET, apart from the above-mentioned components, there exist additional parasitic capacitance components on account of their three-dimensional nature. Considerable work on these additional parasitic capacitances has been done by Wu *et al*. The major additional parasitic capacitance component in FinFETs is the one between the gate and the inner walls of the source, drain, and the access lines. This is shown in [Figure 16].

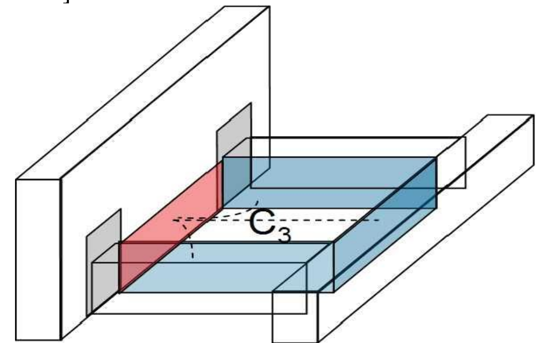

Fig-15:mportant component of a FinFET's parasitic capacitance is the one existing between the gate and the inner walls of the source, drain and the access lines.

The combined effect of the reduced analog transconductance and the increased parasitic capacitance is to degrade the cutoff frequency, f_T, which is proportional to the ratio of the transconductance to the total gate capacitance (which includes the parasitic capacitance). This is shown in [Figure 17].

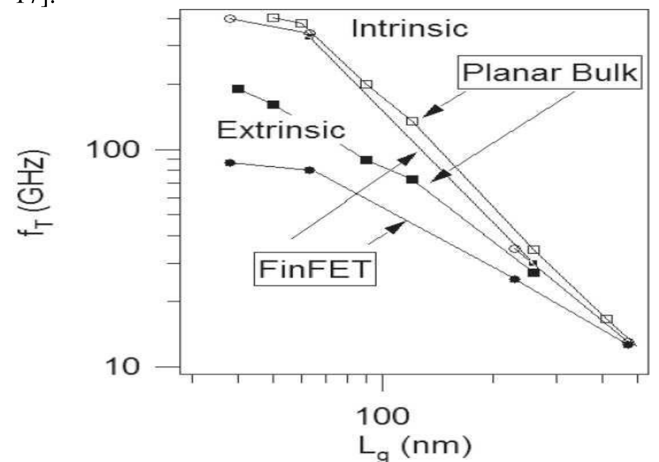

Fig-16: Comparison of intrinsic and extrinsic cutoff frequencies of FinFETs and planar FETs.

While the intrinsic cutoff frequencies of FinFETs is nearly equal to that of planar FETs, the extrinsic cutoff frequency is much reduced owing to higher parasitic capacitances.

4.3 Impact of the Fin Width

An important determinant of the FinFET performance is the width of the patterned width, known as the fin width (W_{fin}). The fin width is very important as it controls the

electrostatics of a FinFET, and thereby it strongly affects its performance.
Going to a narrower fin width increases the electrostatic control of the gate over the channel, thereby suppressing short channel effects and making it possible to scale the channel length even further. From an analog point of view, an increased gate control of the channel translates into a decreased drain control over the channel, resulting in a decreased channel length modulation and lower output conductance (G_{ds}), which is desirable. There are two main drawbacks to decreasing the fin width. The first is the lower electron mobility of the (110) sidewall as compared to the (100) top surface. This can be circumvented by changing the sidewall orientation of nFinFETs. The hole mobility of the (110) sidewall is in fact higher than the (100) orientation; hence, pFinFET performance is expected to be improved compared to planar pFETs. The second drawback to decreasing the fin width is from a technological point of view: it is more challenging to fabricate narrow-width FinFETs on two counts: series resistance and variability. Due to current crowding issues, the series resistance of narrow fins increases dramatically, degrading the drive current and transconductance. Secondly, process-induced variations in the fins become more prominent on going to narrower fin widths. This is known as "fin width roughness" and has a strong negative impact on the device-to-device variability, degrading the mismatch parameters.

4.4 Noise and Mismatch

Noise and mismatch are important considerations for analog and RF applications. The low-frequency (1/f) noise as well as the mismatch is dependent on the quality of the fin wall, which depends on the process-induced roughness. Since there is a strong correlation between fin width and fin roughness, we observe a strong correlation between fin width and the noise/mismatch performance. For extremely narrow fins which suffer from roughness as well as series resistance problems, we see higher noise and mismatch parameters. In the case of FinFETs with somewhat relaxed fin width, we see that the noise is comparable to planar FETs, while the mismatch performance is better. The improved mismatch in this case is attributed to a combination of a lower channel doping and the absence of threshold voltage implants and halo implants in the case of FinFETs.

5.CONCLUSIONS

In conclusion, FinFETs are a promising choice for scaling CMOS into the sub-32 nm era as they are motivated by sound theoretical principles. However, they suffer from the problems of high parasitics and fin roughness. The success of the FinFET technology depends largely on the ability to overcome these two considerable challenges.

REFERENCES

[1]Assaderaghi, S. Parke, D. Sinitsky, J. Bokor, P. Ko, and C. Hu. "A dynamic threshold voltage MOSFET (DTMOS) for very low voltage operation," IEEE Electron Device Lett., vol. 15, no. 12, pp. 510-2, Dec. 1994

[2]M.J. Chen, J.S. Ho, T.H. Huang, C.H. Yang, Y.N. Jou, and T. Wu. "Back-gate forward bias method for low-voltage CMOS digital circuits," IEEE Trans. Electron Devices, vol. 43, no. 6, pp. 904-10, Jun. 1996

[3]Y.K. Choi, T.J. King, and C. Hu. "Spacer FinFET: nano-scale CMOS technology for the terabit era," in Proc. International Semiconductor Device Research Symposium, pp. 543-6, 5-7 Dec. 2001.

[4]Y. Taur, D. Buchanan, W. Chen, D. Frank, K. Ismail, and S.H. Lo, *et al*. "CMOS scaling into the nanometer regime," Proc. IEEE, vol. 85, no. 4, pp. 486-504, Apr. 1997.

[5]H. Wong, K. Chan, and Y. Taur. "Self-aligned (top and bottom) double-gate MOSFET with a 25 nm thick silicon channel," in Proc. International Electron Devices Meeting (IEDM), pp. 427-30, 7-10 Dec. 1997.

[6]T. Skotnicki, J. Hutchby, T.J. King, H.S. Wong, and F. Boeuf. "The end of CMOS scaling: toward the introduction of new materials and structural changes to improve MOSFET performance," IEEE Circuits Devices Mag., vol. 21, no. 1, pp. 16-26, Jan-Feb. 2005

[7]H.S. Wong. "Beyond the conventional transistor," IBM J. Res. and Dev., vol. 46, pp. 133