EFFICIENT RECONFIGURABLE ARCHITECTURE OF BASEBAND DEMODULATOR IN SDR

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Abstract

This paper presents the simulation architecture and performance analysis with the use of ZCD technic. A Zero-Crossing based All-Digital Baseband Demodulation architecture is proposed in this work. This architecture supports demodulation of all modulation schemes including MSK, PSK, FSK, and QAM. The proposed structure is very low area, low power, and low latency and can operate in real-time. Moreover it can switch, in run-time, between multiple modulation schemes like GMSK (GSM), QPSK (CDMA), GFSK (Bluetooth), 8-PSK (EDGE), Offset-QPSK (W-CDMA), etc. In addition, the phase resolution of the demodulator is scalable with performance. In addition, bit-wise amplitude quantization based quad-decomposition approach is utilized to demodulate higher order M-ary QAM modulations such as 16-QAM & 64-QAM, which is also a highly scalable architecture. This structure of demodulator provides energy-efficient and resource-efficient implementation of various wireless standards in physical layer of SDR.

Keywords — *Physical layer, Mobile and Wireless Communication, Software Defined radio (SDR), Zero Cross Detection (ZCD), Modulation Schemes, Architecture, high level synthesis, FPGA.*

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1. INTRODUCTION

Software Radio, by definition, is a class of Reconfigurable radios in which the physical layer behavior can be significantly altered, at run-time, without change in hardware. Thus physical layer reconfigurability is a primary feature of SDR. The Reconfigurable radio can adapt too many different standards and enables global mobility, multi-functionality, compactness and ease of upgrade. The same physical layer can be reprogrammed to support different bands of frequencies, different modulation schemes and different data rates resulting in a significant reduction in product development times and at the same time offering high power efficiency and speed of operations

The architecture choice of physical layer signal processing of a reconfigurable radio is a critical design step. It determines the flexibility, modularity, scalability and performance of the final design. Signal processing algorithms can be implemented using variety of digital hardware such as General Purpose Processors (GPPs), Digital Signal Processors (DSPs), Application Specific Integrated Circuits (ASICs) and Field Programmable Gate Arrays (FPGAs). Where modular design flows are required, FPGAs are preferred over DSPs, as they provide high degree of parallelism and fast interconnections between different modules of a design. FPGA also exhibit high flexibility and reduced design times.

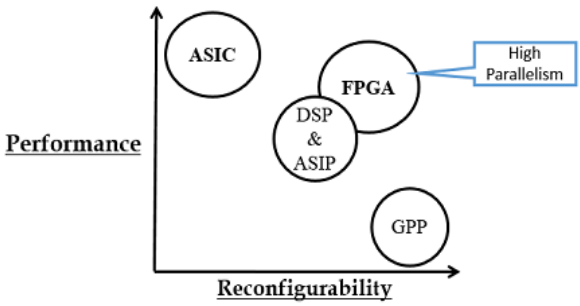

Fig 1.1: Comparison of FPGA, DSP, ASIP, ASIC & GPP for SDR implementation [1]

Hence, FPGAs are highly suitable for efficient implementations of computationally intensive signal processing functions involved in the physical layer of Software Defined Radio, as shown in Figure 1.3. The physical layer involves baseband signal processing which ensures that data received from upper layers, such as MAC, are transferred to the other end of the channel, or recovered, with minimum distortion.

The major functions performed by Physical Layer are as follows:

- Channel Coding- To withstand noise, interference, fading.
- Interleaving- To nullify the effect of burst errors
- Modulation- For bandwidth efficiency & channel transport

2. BASEBAND DEMODULATION

Fundamental Principle of Baseband Quadrature Modulation-Demodulation involves Phase-to-Amplitude Mapping operation at Modulator in Transmitter and Amplitude-to-Phase Mapping operation at Demodulator. The Figure 2.2 depicts the flow of operations involved in Modulator.

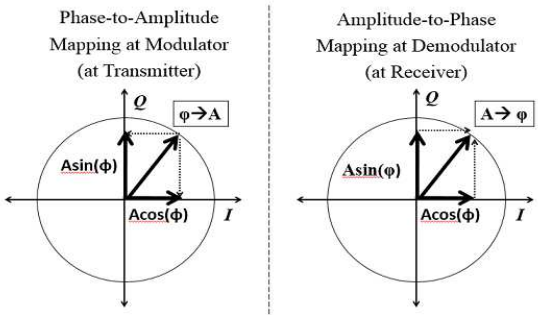

Fig 2.1: Fundamental Principle of Baseband Quadrature Modulation-Demodulation

At receiver end, Amplitude-to-Phase Mapping at Demodulator. The Figure 2.3 shows the flow of operations involved in Demodulation. At the receiver end, phase recovery is essential for demodulation. The digital demodulation algorithms can be primarily classified into two categories depending on the phase accuracy requirements:

- Modulations which require accurate Phase Reconstruction at Receiver for efficient Symbol Recovery
  - includes - GMSK, GFSK, DQPSK, 8-DPSK, 8-PSK
  - all these schemes are very robust to channel e_ects like AWGN, phase distortion,inter-symbol interference, fading, etc.
- Modulations which directly operate on I & Q values and thus does not require highly accurate Phase Reconstruction for Symbol Recovery
  - includes - QPSK, Offset-QPSK, BPSK, DBPSK, 16-QAM, 64-QAM
  - not very robust to channel effects

Conventional techniques for Phase Reconstruction require Co-ordinate Rotation Digital Computer (CORDIC) which has generally a word-parallel n-stage pipelined architecture.

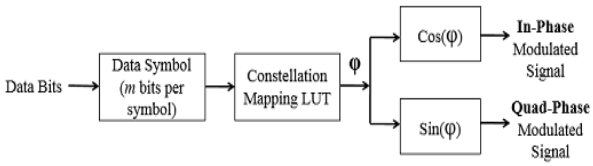

Fig 2.2: Phase-to-Amplitude Mapping at Modulator (Transmitter) [3]

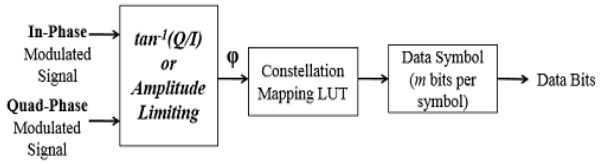

Fig 2.3: Amplitude-to-Phase Mapping at Demodulator (Receiver) [3]

3. ACCURATE PHASE RECONSTRUCTION USING ZERO-CROSSING DETECTION

Phase Reconstruction can be achieved by performing linear addition/subtraction combinations of In-phase and Quad-phase signals into generating several phase axes at a definite angle in phase domain. The zero-crossing detection technique has scalable phase accuracy, i.e. the phase resolution can be increased by increasing the number of phase axes by adding more addition units. This technique is realized by a purely combinational logic, therefore enables very high speed Phase Recovery.

The following are the advantageous features of zero-crossing detection base phase recovery, as compared to CORDIC based phase recovery:

- Scalable phase accuracy
- Realized by combinational logic
- Very high speed
- Well suited to Non-Coherent Demodulation
- Phase-Locked Loop not required
- Very low design complexity compared to CORDIC

Zero Crossing based Quadrature baseband demodulation was first proposed by E.K. B. Lee at Motorola in 1995 [6] and later on improved by S. Samadian at UCLA in 2003 [7]. However the implementation of Phase Axes Generator proposed by the above author involved analog circuit components like operational-amplifiers for scaling and addition in analog domain. Presence of opamps in the receiver circuit drastically increases the area occupied and the power consumption of the receiver. Therefore, to eliminate analog components, an all-digital Phase Axes Generator is proposed in this work, which is connected in series with a standard Analog-to-Digital converter circuit. Thus the entire demodulation operation is performed in digital domain.

In the proposed demodulator, the phase axes generator module is implemented completely in digital domain and no scaling multiplication/division operations are required. This allows highly area efficient and timing efficient, low power, implementation of demodulator on FPGA.

In the first step, multiple phase axes are generated in phase domain by linear combination of received I and Q baseband signals. A tree of adders produces multiple phase axes, where

first column of adders produce phase axes at 45 degrees and next column of adders produce a phase axes at 22.5 degrees. Thus phase resolution can be linearly increased with increase in adders

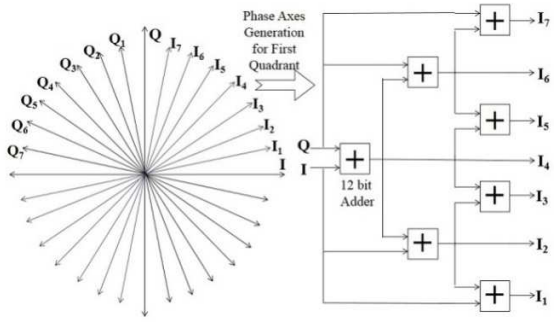

Fig 3.1: Phase Axes Generation Circuit for First Quadrant of Phase Domain I-Q Plane

Thus total 14 adders are required to generate 14 extra axes (apart from I and Q) in the phase domain I-Q plane, dividing the phase domain in total 32 sectors resulting in a phase resolution accuracy of 360/32 = 11.25 degrees. For tracking the instantaneous phase of the input I-Q modulated signals, the MSB of each of the phase axes is considered to represent a thermometer code Indicating the current phase position of the input modulated signal, as shown in Figure. The thermometer code so obtained is further encoded to binary representation of 5 bits (for total 32 sectors) by a look-up table. In this way the instantaneous phase of the modulated signal is tracked by zero-crossing detection in MSB of multiple phase axes signals.

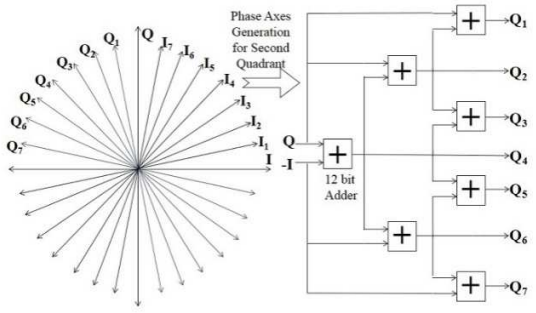

Fig 3.2: Phase Axes Generation Circuit for Second Quadrant of Phase Domain I-Q Plane

4. SIMPLER DETECTOR BASED ON PHASE ENCODING

Instead of sensing phase rotation by counting crossings across reference axes, a more direct way is to read the instantaneous phase from the 16-bit thermometer code at the output of the comparator array [Fig. 4.1]. With eight 1-bit zero-crossing detectors, this code resolves the instantaneous phase to an accuracy of. For example, the code corresponding to the shaded segment in Fig. 5(b) is 0000 1111 1111 1111; as the phase of the GFSK vector rotates clockwise from the shaded segment to the striped segment, the code changes to 0000 0111 1111 1111, whereas if the vector rotates counterclockwise to the dotted segment, the code becomes 0001 1111 1111 1111.

The demodulator needs only to know the initial and final values of the code across one symbol period to determine the angle of the received waveform and the direction of rotation. This simplifies the circuit considerably. Although for timing synchronization it is necessary to oversample the down converted signal, this simple detector itself clocks at the symbol rate, 1 MHz, which lowers power consumption.

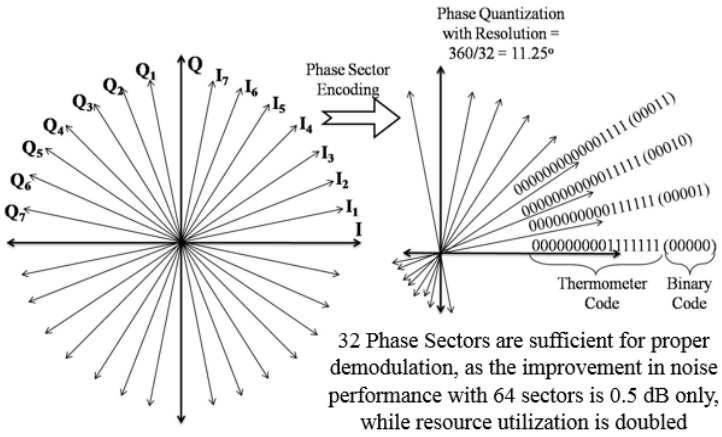

Fig 4.1: Phase Sector Encoding for Instantaneous Phase Tracking of the incoming signal

5. THE NOVEL POST PROCESSING CIRCUIT

A novel post-processing circuit is proposed for all demodulators corresponding to all modulation schemes. The proposed circuit improves BER performance of demodulator by detecting a stable symbol at the output of demodulator. The circuit parameters include:

i. Oversampling factor (N) for the modulation scheme. Generally, N = 8.
ii. Symbol word size (m), i.e. no. of bits representing one symbol in constellation of the modulation scheme.

The circuit operates on the following principle: "A symbol is Output, if and only if, it is detected at the demodulator output continuously for ((N/2) +1) clock cycles, otherwise continue previous symbol at output"

Where N = no. of samples per symbol (oversampling factor specified by a wireless standard, a common characteristic of both modulator and demodulator).

The proposed stable symbol detection circuit is shown in Figure 5.1. This novel circuit is implemented for all demodulators designed in this work.

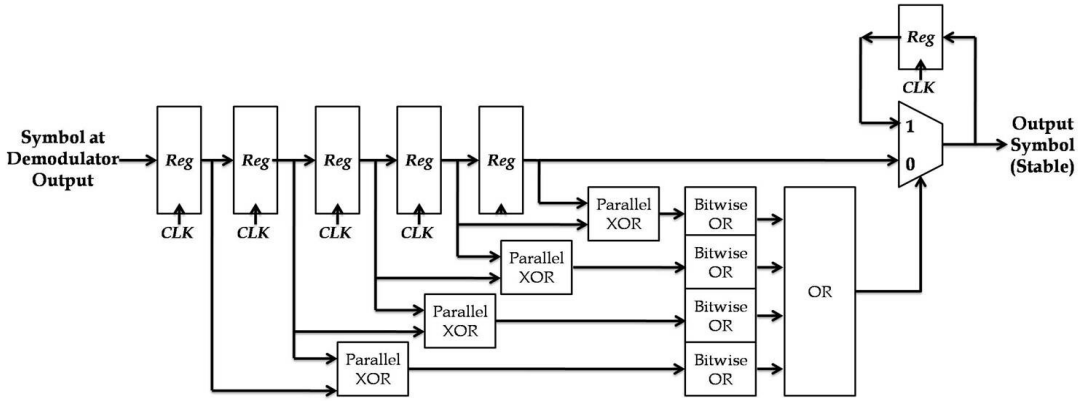

Fig 5.1: Proposed Stable Symbol Detection Circuit

6. EXPERIMENTAL RESULTS

In the proposed demodulator for GSM (we can take any Wireless Standard), the phase axes generator module is implemented completely in digital domain and no scaling multiplication/division operations are required. This allows highly area efficient and timing efficient, low power, implementation of demodulator on FPGA.

In the first step, multiple phase axes are generated in phase domain by linear combination of received I and Q baseband signals. A tree of adders produce multiple phase axes, where first column of adders produce phase axes at 45 degrees and next column of adders produce a phase axes at 22.5 degrees. Thus phase resolution can be linearly increased with increase in adders.

In the second step, zero crossings are detected in the multiple phase axes signals by representing them in 2's complement signed integer format. Here the MSB of the signal contains zero-crossing information.

The zero crossing information obtained from previous block is given to a thermometer encoder which allows us to represent the current position of the incoming phase signal in a phase domain. Thus each phase sector is assigned a thermometric code.

The thermometric code is converted to binary code representation which allows us to determine the difference in phase between consecutive sectors while the incoming signal moves along the axes.

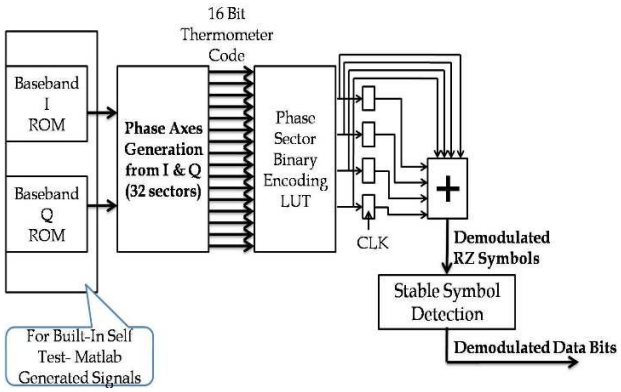

Fig 6.1: Proposed GMSK Demodulator based on Zero-Crossing Phase Reconstruction and Stable Symbol Detection Post-Processing

6.1 Phase Reconstruction Module Synthesis Results:

The HDL code for each IP was implemented in Xilinx ISE and the resource utilization and static timing afinalysis were noted. For comparison, standard parameterizable IP cores from Xilinx LogiCORE generator were considered for resource utilization assessment.

In case of demodulation, typically a arctangent function is required for performing amplitude-to-phase conversion or phase reconstruction. Therefore a standard atan word-parallel CORDIC algorithm IP from LogiCORE generator was synthesized and the resource utilization were compared with the resource utilization of the phase reconstruction module employed in the proposed demodulator structure. It is observed from Table 6.1 that the resource utilization for phase reconstruction module is nearly one-half of the CORDIC resource utilization.

Table 6.1: Comparison of Resource Utilization between proposed Zero-Crossing based Phase Reconstruction module and CORDIC IP from Xilinx LogiCORE Gen-serator

Resource Utilization	Proposed Zero-Crossing Based Phase Reconstruction	CORDIC IP from XlinikLogicCORE
Slice Registers	15	311
Slice LUTs	274	527

Moreover, the latency of CORDIC is N clock cycles where N is equal to the number of pipeline stages in CORDIC. On the other hand, the phase reconstruction module in proposed demodulator is purely combinational logic therefore latency/delay is very very less compared to the CORDIC.

In terms of complexity, CORDIC requires pre-computation of coefficients prior to synthesis, according to the phase accuracy requirements. This leads to high accuracy of phase reconstruction, nearly 0.1 degrees, as compared to 11.25 degrees for the proposed demodulator. However, experimentally it is found that very high accuracy of phase reconstruction is not necessary when a moderate modulation index is specified in the standard. For example, in GSM, the GMSK modulation index is 0.5 which results in 90 degrees change in phase for one change in symbol. This 90 degrees change can be efficiently detected by 11.25 degree phase resolution and higher phase resolution is not required. Similarly, in Bluetooth, the GFSK modulation index specified is 0.28 to 0.35 which is nearly 60 degrees phase change, which can also be efficiently detected by 11.25 degrees phase resolution.

7. CONCLUSIONS

It was observed that the above mentioned algorithms significantly reduce the complexity of the receiver architecture and thus enable a resource-efficient, low latency, low delay, low power, all-digital implementation on FPGA. At the same time, there is some minor degradation in Bit Error Rate (BER) performance as compared to the theoretical "ideal demodulator". However this trade-off is very much in favor of low cost, low complexity, flexible receivers which are widely employed in modern communication devices.

Zero Crossing based Baseband Demodulation, General Approach for Multi-standard Demodulation Novel Post-processing circuit, with Stable symbol detection, for all Demodulators to improve BER and All-Digital Phase Axes Generation Scalable, Low Complexity, Hierarchical Adder based circuit.

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