DESIGN OF VCO USING CURRENT MODE LOGIC WITH LOW SUPPLY SENSITIVITY

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Abstract

The function of an oscillator is to convert dc energy into RF. Voltage Controlled Oscillator (VCO) is a type of oscillator whose output frequency can be varied by a control voltage. Here the VCO is designed using 0.18µm CMOS-RF technology using current mode logic. The Current mode logic is the fastest logic and is mainly used in Clock and Data Recovery applications. Current mode logic (CML) is a differential logic and provides noise immunity. Using the proposed design the current mode logic VCO operates with a supply voltage of 1.8 V and frequency varies from 2 MHz to 2.5 MHz. Its normalized supply sensitivity is 0.976 and optimum sensitivity is 0.966.

Keywords: *VCO, Supply sensitivity, CML, Ring oscillator.*

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1. INTRODUCTION

A Voltage Controlled Oscillator (VCO) is one of the important blocks in PLL, Transceivers, and CDR circuits. Its main function is to generate output frequency of desired range with respect to the input control voltage. The analog performance of oscillators also suffers from the noise induced on the power supply due to switching of internal digital sub circuits. This particularly affects the ring oscillators. LC oscillators exhibit very low supply sensitivity because their oscillation frequency is determined by passive capacitor and inductor. But ring oscillator based VCOs are preferred because they are area efficient.

There are varieties of techniques to limit the power supply sensitivity. Some of them are: The supply voltage itself is used as control voltage. A source follower is used instead of dc current source to couple the control voltage to differential pair, which makes biasing less robust. A clean supply and ground pad in the VCO requires additional pins which may not always be available. The supply is regulated with a low drop-out regulators causes increase in power dissipation due to extra circuitry and higher supply voltage. Another method uses a compensation technique where bias current and voltage swing are controlled simultaneously.Digital calibration technique works better for CMOS ring oscillators to reduce supply sensitivity because their frequency range is less compared to current mode logic ring oscillators.

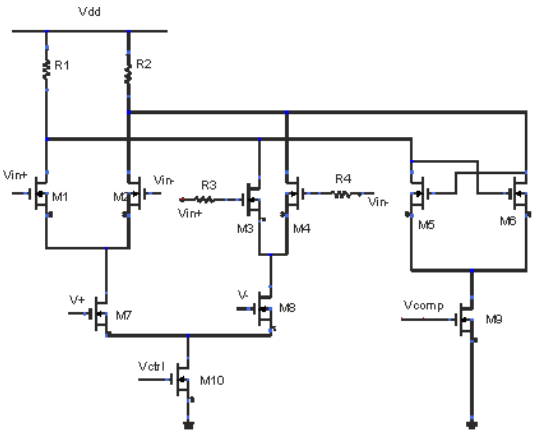

Fig. 1.Single stage delay cell in proposed VCO

Current mode logic is a differential logic style and it has many advantages like low noise level generation and noise immunity. The amount of current drawn from the power supply does not depend on switching activity. So it is useful in analog and mixed signal integrated circuits. Current mode logic circuits have high current swing with low supply voltage, low input impedance, high output impedance, reduced distortion and better ESD immunity.

2. CIRCUIT TOPOLOGY

There are many topologies to design the VCO. Some of them are LC oscillator based VCO, Ring Oscillator based VCO and Relaxation oscillator based VCO. Supply sensitivity is a measure of the effect of variation of the supply voltage on the response of the circuits. It is defined by the percentage change

in oscillation frequency to the percentage change in supply voltage. Supply sensitivity decreases with increase in frequency. At higher operating frequencies, sensitivity falls below zero to a negative value[1].

LC Oscillator based VCO has high frequency and phase stability but harder to integrate in ICs and occupies more area. Tuning range is also very less. However, they are very less sensitive to supply voltage because their oscillation frequency depends on inductor and varactor [7]. Relaxation oscillator based VCOs require only single reactive element to make oscillations. These can be easily fabricated as ICs. Even though these types of VCOs have wide tuning range, they cannot generate pure sinewaves. At high frequencies, they have poor frequency stability and phase noise is also high [5]. Ring oscillator based VCOs are easy to integrate in ICs [3]. CMOS VCO based on a ring oscillator has positive supply voltage sensitivity for most of the operating frequencies [6]. So the output frequency increases as the supply voltage increases. But the frequency range is higher in CML based VCOs. The main advantage of Ring oscillator based VCOs are, they take up small layout area and the tuning range is wider compared to LC oscillator based VCOs. CMOS Ring oscillators based VCOs are slow compared to CML VCOs and susceptible to more jitter. In high speed circuits, differential signals are used so that a compact design and better noise immunity can be achieved. This principle is used in current mode logic circuits. Ring oscillator based CMOS VCOs are more sensitive to supply voltage compared to LC oscillator based VCOs. By adding a compensation circuit, supply sensitivity is greatly reduced. The purpose of compensation circuit is to make the VCO insensitive to supply voltage. By adding the compensation circuit at the end of each stage in delay cell, area is increased slightly and power consumption is also increased.

3. CIRCUIT DESCRIPTION

The proposed design contains 4 stage delay cells and a single delay stage is shown in figure 1, which is connected in cascade in order to make a ring oscillator based voltage controlled oscillator. At the end of each stage, compensation circuit is added to reduce the supply sensitivity. Compensation circuit is shown in Fig.2.In this circuit, the transistor drain voltages follow the variations of Vdd, the current Icomp also increases as does gm in M5 & M6. Thus the differential admittance of the compensation circuit becomes more negative as Vdd increases. If this circuit is connected in parallel with a CML delay cell, it could thus provide compensation for the supply variation. A shorter delay is realized by transistor M1 and M2 while a longer delay is realized by resistors R3 & R4 with transistors M3 & M4. The overall delay is tuned with V+-V- which realizes a weighted sum of the faster and slower delays, while keeping the power and amplitude constant.By varying the supply voltage and control voltage (Vctrl), the output frequency is varied. Vctrl is applied to transistor M10. It has a wide tuning range from 0.7 to 1.8 V. The typical values of the resistors and transistors are given in the table 1.

Table 1. Component values

Transistors	(W/L) all µm	Resistors	In Ω
M1-M4 M5-M6 M7-M8 M9 M10	2.4/0.18 34/0.18 1.7/0.18 13/3.6 72/3.6	R1-R2 R3-R4	400 1000

4. RESULTS AND DISCUSSIONS

The VCO using current mode logic was simulated using Advanced Design System (ADS). Fig 3 shows the simulated gain of the design and Fig 5 shows the simulation results of the input return loss of the proposed design. Fig 4 shows the transient response of the VCO. Table 2 gives the sensitivity analysis of the proposed design.

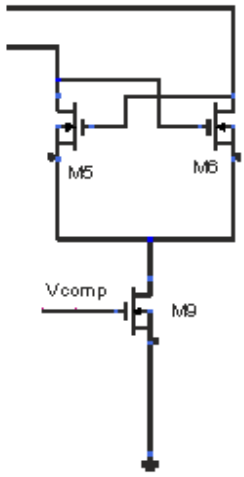

Fig. 2 Compensation circuit

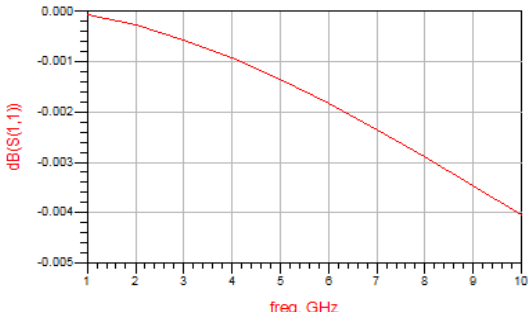

Fig 3 Simulated input return loss (S11) of proposed design

Table 2 Sensitivity Analysis of the proposed design

Sens Variable	Norm_vo	Optim1_vo
Supply voltage	0.976	0.966

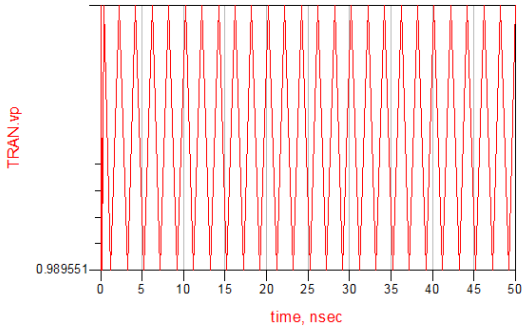

Fig 4 Transient response of the proposed circuit

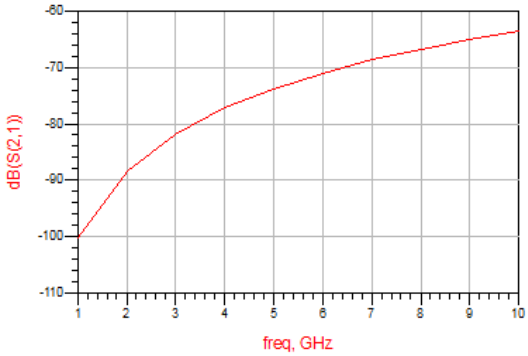

Fig 5 Simulated gain (S21) of proposed design

Table 3 Performance summary and comparison with other CML circuits.

	Supply Voltage (V)	Frequency Range (in GHz)	Power Dissipation (mW)	Normalised Sensitivity	Optimum Sensitivity
[3] Ring Oscillator	1.8	2.2-2.7	10.1	1.002	0.991
This work (VCO)	1.8	2-2.5	5.56	0.976	0.966
[1] Ring oscillator (without compensation)	1.8	2.2-2.7	10.1	2	1

5. CONCLUSIONS

In this paper, a Voltage Controlled Oscillator using current mode logic was designed using 0.18µm CMOS technology. It has a wide tuning range from 0.7 to 1.8V and the frequency varies from 2 -2.5 GHz.

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