# STUDY AND IMPLEMENTATION OF COMPARATOR IN CMOS 50NM TECHNOLOGY

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#### Abstract

This paper describes the comparator circuits used in FLASH Analog to digital converter (ADC). The performance of FLASH ADC is greatly influenced by the choice of comparator. In this paper, first a single ended "Threshold Inverter Quantizer" (TIQ) is presented. The TIQ comparator is based on a CMOS inverter cell, in which voltage transfer characteristics (VTC) are changed by systematic transistor sizing. However, TIQ comparator is very sensitive to power supply noise. Another comparator circuit presented in this paper is "Two stage open loop comparator". It is implemented in 50 nm CMOS Technology. Pre-simulation of comparator is done in LT-Spice and post layout simulation is done in Microwind 3.1.

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# **1. INTRODUCTION**

The comparator is a circuit that compares one analog signal with another analog signal or a reference voltage and outputs a binary signal based on the comparison [1,2]. Comparator is the "Heart" of the Analog to digital converter. The comparator is basically a 1-bit analog-to-digital converter. Fig. 1 shows general block diagram and Fig. 2 shows symbol of comparator.



Fig -1: Block diagram of a comparator



Fig -2: Symbol of a comparator

The comparator is a critical part of almost all kind of analogto-digital (ADC) converters. Depending on the type and architecture of the comparator, the comparator can have significant impact on the performance of the target application. The speed and resolution of an ADC is directly affected by the comparator input offset voltage, the delay and input signal range. Some basic applications of comparators are analog-to-digital conversion, function generation, signal detection and neural networks etc.

The following study gives an overview of some of the different comparator topologies examined during the prestudy. Here, first TIQ comparator is described. TIQ comparator has single ended input and reference voltages are changed where there is a noise in the power supply voltage. Then Two stage open loop comparator is presented in this paper.

This paper is organized into four sections. Section 2 deals with the design of TIQ comparator. Section 3 discuss "Two stage open loop comparator" and section 4 gives simulation results of the two stage open loop comparator.

# 2. TIQ COMPARATOR

The use of two cascading inverters as a voltage comparator is the reason for the technique's name. The voltage comparators compare the input voltage with internal reference voltages, which are determined by the transistor sizes of the inverters. Hence, we do not need the resistor ladder circuit used in a conventional flash ADC. Comparator's role is to convert an input voltage (Vin) into a logic `1' or `0' by comparing a reference voltage (Vref) with the Vin. If Vin is greater than Vref , the output of the comparator is `1', otherwise `0'. The TIQ comparator uses two cascading CMOS inverters as a comparator for high speed and low power consumption as shown in Fig. 3. The inverter threshold (Vm) is defined as the Vin = Vout in the Voltage Transfer Characteristics (VTC) of an inverter as shown in Fig. 4. We can set inverter threshold voltage from following equation:

$$V_{m} = (r(V_{dd} + |V_{tp}|) + V_{tn}) / (1+r)$$

with  $r = (k_p/k_n)^{1/2}$ 



Fig -3: TIQ Comparator



Fig -4: Voltage Transfer characteristic curve

Where Vtn and Vtp are the threshold voltages for NMOS and PMOS devices, respectively.

$$\begin{split} K_n &= (W/L)n \;.\; \mu_n \; C_{OX} \\ K_p &= (W/L)p \;.\; \mu_p \; C_{OX} \end{split}$$

The second inverter is used to increase voltage gain and to prevent an unbalanced propagation delay [4]. With a fixed length of the PMOS and NMOS devices, we can get desired values by changing only the width of the PMOS and NMOS transistors. We assume that both transistors are in the active region, the gate oxide thickness (Cox) for both transistors are same, and the lengths of both transistors (Lp and Ln) are also the same. So, Vm is shifted depending the transistor width ratio (Wp/Wn). That is, increasing Wp makes Vm larger, and increasing Wn results in Vm being smaller on the VTC.

However, to use the CMOS inverter as a voltage comparator, we should check the sensitivity of Vm to other parameters, which are ignored for correct operation of the TIQ comparator. In a mixed-signal design, the ignored parameters threshold voltages of both transistors, electron and hole mobility, and power supply voltage - are not fixed at a constant value. There are some main disadvantages of the TIQ approach:

1. It is a single-ended structure.

2. It requires a separate reference power supply voltage for analog part only due to poor power supply rejection ratio.

3. It has slight changes in linearity measures (DNL, INL) and the maximum analog input signal range due to process parameter variations. These problems can easily be handled by front end signal conditioning circuitry.

4. It requires a S/H at the analog input to increase the performance and to reduce the power consumption during metastable stage.

# 3. TWO STAGE OPEN LOOP COMPARATOR

In previous section, we have seen comparator circuits which generates references voltages internally based on transistor size. Now, in this section, we will study about two stage open loop comparator circuit which has two differential inputs. This comparator consists input stage, differential amplifier and output stage as shown in Fig. 5. The advantage of this circuit is that the circuit consumes minimal number of transistor and thus the circuit area is small [5].



Fig -5: Two stage open loop comparator

The two-stage op amp without compensation is an excellent implementation of a high-gain, open-loop comparator [2]. Comparator requires differential input and sufficient gain to be able to achieve the desired resolution. So, two stage op-amp makes an excellent implementation of the comparator. A simplifications occurs because comparator will generally be used in an open loop mode and therefore it is not necessary to compensate the comparator. In fact, it is preferred not to compensate the comparator so that it has the large bandwidth possible, which will give a faster response.

The first item of interest is the values of VOH and VOL for the two stage comparator. Since the output stage is a currentsink inverter, maximum output voltage can be expressed as,

$$V_{OH} = V_{DD} - (V_{DD} - V_{G6}(\min) - |V_{TP}|) \left[ 1 - \sqrt{1 - \frac{8I_7}{\beta_6 (V_{DD} - V_{G6}(\min) - |V_{TP}|)^2}} \right]$$

The minimum output voltage is

$$VOL = VSS.$$

We can design two stage open loop comparator from following formulas:

$$(W_6/L_6) = (2I_6)/(K_p * (V_{SD6(sat)})^2);$$
  

$$(W_7/L_7) = (2I_7)/(K_N * (V_{DS7(sat)})^2);$$
  

$$(W_3/L_3) = (W_4/L_4) = (I_5)/(K_p * (V_{SG3} - |V_{TP}|)^2);$$
  

$$(W_1/L_1) = (W_2/L_2) = g_{ml}^2/(K_N * I_5);$$

 $(W_5/L_5) = (2I_5)/(K_N^{*}(V_{DS5(sat)})^2);$ 

Where,  $I_6 = I_7 = (|P_{11}| * C_{11})/(\lambda n + \lambda p);$ 

$$\begin{split} |\mathbf{P}_{11}| &= 1/(t_p*(mk)^{1/2}) ; \\ \mathbf{I}_{5} &= (2*\mathbf{I}_{7}*\mathbf{C}_{1})/\mathbf{C}_{11}; \end{split}$$

#### **4. SIMULATION RESULTS**

In this section, the functional and post-layout simulation results of the two stage open loop comparator have been presented. There are two parts of result. First, functional simulation of comparator is done in LT-Spice software using 50 nm CMOS technology. Then, post-layout of comparator is done in Microwind 3.1 using 50 nm CMOS technology.

#### **4.1 Functional Simulation**

Table 1 denotes the short-channel MOSFET parameters for general analog design with a scale factor of 50 nm (scale=50e<sup>-9</sup>). In Fig. 5, a proposed comparator circuit is shown. The frequency of the analog signal input is varied in the way that the minimal propagation time delay is obtained. For the functionality purpose as shown in Fig. 6(a), the reference voltage, Vref is set to 0.8V and the supply voltage is 1.1V. As illustrated in Fig. 6(a), if the input voltage is higher than 0.8V, the output of comparator is high and vice versa. Same way, in Fig. 6(b), Vref is set to 0.4V.

 Table -1: MOSFET model parameters for 50nm CMOS

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Short-Channel MOSFET parameters		
<i>VDD</i> =1.1V and a scale factor of <b>50 nm</b>		
Parameter	NMOS	PMOS
Bias Current, $I_D$	10µA	10µA
$V_{DS,sat}$ and $V_{SD,sat}$	50 mV	50 mV
$V_{GS}$ and $V_{SG}$	350 mV	350 mV
$V_{THN}$ and $V_{THP}$	280 mV	280 mV
$v_{satn}$ and $v_{satp}$	$110 \times 10^3$ m/s	$90 \times 10^3 \text{ m/s}$
T <sub>ox</sub>	14Å	14Å
C' <sub>ox</sub>	$25 f F/\mu m^2$	$25 f F/\mu m^2$



Fig -6: Output of a comparator (a) Vref = 0.8V (b) Vrf = 0.4V

#### 4.2 Layout of Comparator

Since, the design automation for analog and mixed signal circuits has not evolved as much as its digital counterpart; thereby designers are often forced to do the full-custom designs. Thus it is still a designer's experience that produces effective transistor sizing and layout strategies. A fully systematic approach for producing an optimal analog layout is something that is still under development. The layout of the Comparator is done with the primary objective of reducing the area overhead to an optimum level, while maintaining a simplistic approach. Fig. 7 shows layout of proposed comparator using 50 nm with 0.7V power supply. For the functionality purpose as shown in Fig. 8, the reference voltage, Vref is set to 0.5V. As illustrated in Fig. 8, if the input voltage is higher than 0.5V, the output of comparator is high and vice versa [9].



**Fig -7**: Layout view of a comparator



Fig -8: Output of a comparator

# **5. CONCLUSIONS**

In this paper, a comparator circuit is proposed. There are some disadvantages of TIQ comparator in some applications as stated in section 2. Two stage open loop comparator is presented using 50nm CMOS technology. This architecture can be extended to medium-to-high resolution applications because the simplicity of the circuit. Comparator is a main part of flash ADC. As a future work, we can design low power flash ADC using this comparator design.

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