ESTIMATION AND DESIGN OF MC-DS-CDMA FOR HYBRID CONCATENATED CODING IN HIGH SPEED VEHICULAR COMMUNICATION

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Abstract

The design of Multi Carrier Direct Sequence Code Division Multiple Access (MC-DS-CDMA) structure which generalizes serial and parallel concatenated code is investigated to this project. This model is ideal for designing various codes in the performance of both error floor and water floor region. We propose a concatenated code for transmitter block which is used for multi carrier direct sequence CDMA technique. Simulation results of MC-DS-CDMA uplink system using Cadence software shows the various parameters such as memory, Execution time and number of transient steps required for the Execution of MC-DS-CDMA uplink system was estimated and also power consumed was determined for each block in the transmitter. An improved concatenated code model is used for uplink mobile communication. Further system performance improvements can be obtained by concatenating inner code and outer code and the results of computer simulations demonstrate that the performance of the concatenated code was investigated.

Keywords: *Code Division Multiple Access, Concatenated code, inner code, outer code, interleaving and power analysis.*

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1. INTRODUCTION

The enormous growth of wireless mobile communication systems will be required to support high speed transmission rate, high performance, high capacity and high bit rate. The modern communication system integrates voice, images, data and video signals. Recently, the combination of OFDM and CDMA gives the new advance technique known as MC-DS-CDMA.

A Fourth Generation of Wireless communication makes use of this Multi Carrier Direct Sequence Code Division Multiple Access (MC-DS CDMA) system [1]. The MC-DS-CDMA requires the advantage of synchronization between transmitter and receiver particularly for uplink which cannot be estimated in the presence of fading channel. MC-DS-CDMA has the highest degrees of freedom in the family of CDMA schemes.

The generalized class of concatenated convolutional codes based on union bounds for the error probability and extrinsic information transfer (EXIT) charts for the decoding threshold are performed [2]. To increase the number of users and combined with a user-grouping technique and reduce the effects of multiuser interference[3]. A novel logarithmic likelihood ratio (LLR) post processing Technique was used. Multiple parallel concatenated code with curve-fitting technique is used for turbo codes [4].

The main purpose of multiple access schemes are used to achieve several number of users to access the same channel without any mutual interference problem in it. The design of low complexity rate –compatible code and it provides both serial and parallel concatenated codes. Lower error floors and high code rates are obtained [5]. The serial to parallel converted data streams' using a given spreading code and then modulates a different subcarrier with each of the data stream. This Paper is organized as follows. The design of MC-DS-CDMA system and concatenated code are given in section II. In section III, the results are discussed. Section IV, Concludes the paper and Section V gives the Acknowledgement.

2. MC-DS-CDMA SYSTEM DESIGN FOR TRANSMITTER MODEL

The multi carrier DS-CDMA transmitter spreads the Serial to-Parallel converted data streams using a given spreading code in the time domain. So, that the resulting spectrum of each subcarrier can satisfy the orthogonality condition with the minimum frequency separation

2.1 TF-Domain Of MC-DS-CDMA Model

In Multi Carrier Direct Sequence Code Division Multiple Access system the same bandwidth was shared by different users. Due to that Multi user Interference will occur. The MUI is introduced at the receiver part due to the propagation delay difference between different users and also due to the cross-correlation properties of different users at the time- domain spreading sequences. This scheme is originally proposed for a

uplink communication channel, because the introduction of OFDM signaling into DS-CDMA scheme is effective for the establishment of a quasi-synchronous channel. The transmitter section of this MC-DS-CDMA is given by the generalized block diagram as shown below.

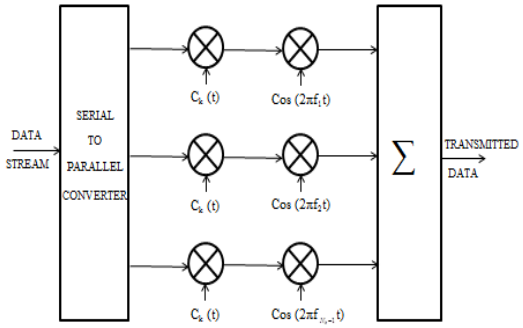

Fig 1: MC-DS-CDMA Transmitter Model

The MC-DS-CDMA signal is generated by serial-to-parallel converting data symbols into Nc sub-streams and applying DS-CDMA on each individual sub-stream. With MC-DSCDMA, each data symbol is spread in bandwidth within its sub-channel, but in contrast to MC-CDMA or DS-CDMA not over the whole transmission bandwidth for Nc > 1. An MC-DS-CDMA system with one sub-carrier is identical to a single-carrier DS-CDMA system.

MC-DS-CDMA is of special interest for the asynchronous uplink of mobile radio systems, due to its close relation to asynchronous single-carrier DS-CDMA systems. Figure1. shows the generation of a multi-carrier direct sequence spread spectrum signal. The data symbol rate is 1/Td . A sequence of Nc complex-valued data symbols dn(k), n = 0, . . ., Nc − 1, of user k is serial-to-parallel converted into Nc sub-streams.

2.2 Concatenated Code Model

Concatenating two convolutional codes in series gives serially concatenated convolutional codes (SC turbo codes). We arrive at turbo block codes by concatenating two block codes and at repeat–accumulate codes by concatenating a repetition code and a convolutional (accumulator) code.

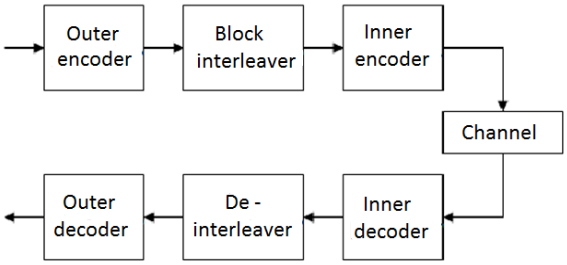

Fig2: Concatenated Code model

The code rate of a systematic SC code with a rate r1 = k1/n1 inner code and a rate r2 = k2/n2 outer code is ,

$$K/n = k1/(k1+n2) = k1/(k1+n1/r2) = r1r2/(r1r2+1) \quad (1)$$

From Equation (1), serial concatenation with a rate kO/nO outer convolutional code and rate kI/Ni inner convolutional code, a fixed-length-K message is encoded. The outer code can thus be considered as an (NO = KnO/kO , KO = K, dmin(O)) block code and the inner code as an (NI = KInI/kI, KI = NO, dmin(1)) block code. Using a length NO = KI interleaver, the concatenated code is thus an
(N = NI, K = KO, dmin) block code.

2.3 Serial Concatenated Code

The first serial concatenation schemes concatenated a high-rate block code with a short convolutional code. The first code, called the outer code, encoded the source message and passed the resulting code word to the second code, called the inner code, which re-encoded it to obtain the final code word to be transmitted.

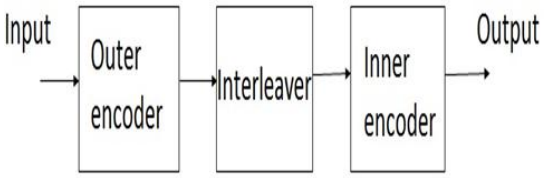

Fig3: Serial Concatenated code model

At the decoder the inner code decoded the received sequence from the channel and passed its decoded message to the outer code, which used it to decode the original source message. An interleaver was used between the two codes to spread out any burst errors produced by the inner decoder.

2.4 Interleaving

Signals traveling through a mobile communication channel are susceptible to fading. The error-correcting codes are designed to combat errors resulting from fades and, at the same time, keep the signal power at a reasonable level.

Most error-correcting codes perform well in correcting random errors. However, during periods of deep fades, long streams of successive or burst errors may render the error-correcting function useless.

3. RESULTS AND DISCUSSIONS

Simulation output is to be obtained by using CADENCE in analog design. In this Multi Carrier Direct Sequence CDMA transmitter block was designed. For the transmitter modulation scheme of BPSK modulation schematic diagram was

designed. In this the transient response are obtained. Figure4 shows the overall output of the BPSK modulator.

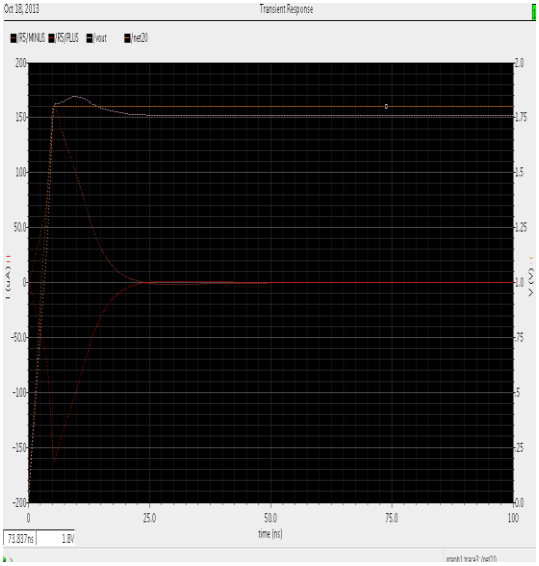

Fig4: Simulation output of BPSK modulator

The current and voltage measurements are shown by Figure5 which is should be used on the transmitter block of BPSK modulator. Where maximum of 1.8 v should be given to each vpulse of the source input.

The inputs are given to each resistance and transistors and assign the vpulse as 1.8 v and choose the transient response model and give the required parameters. After to select the schematic of vdc or any other parameter and simulate the circuit.

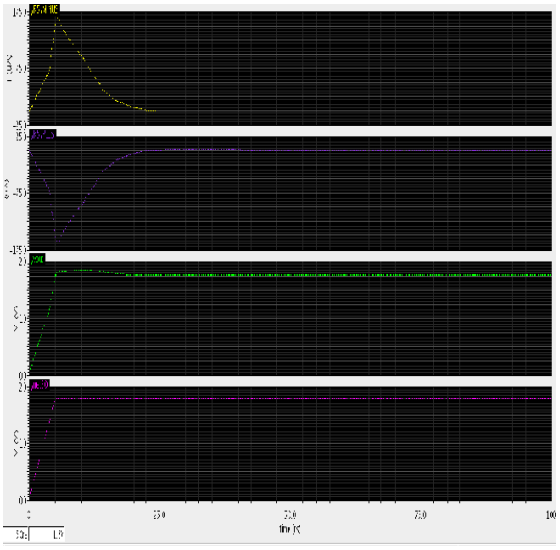

Fig5: Transient response of BPSK modulator

The overall power of the circuit is obtained by transient analyzes. Figure6 shows the total power obtained by the BPSK modulator. The overall power for the modulator is 2.23 mw.

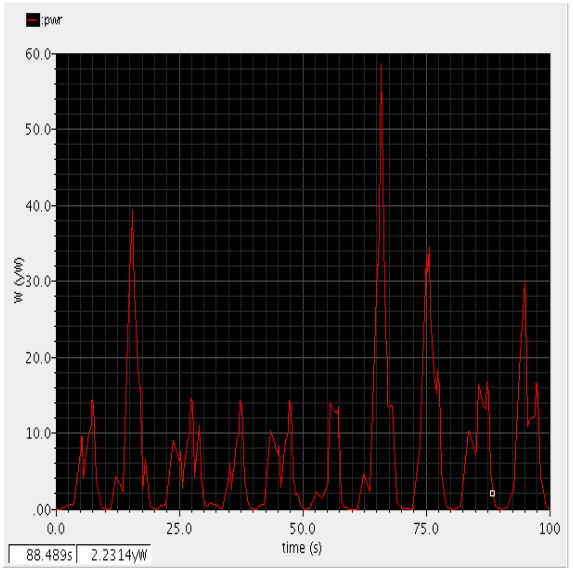

Fig6: Simulation of power output BPSK

Next the simulation output of channel model was obtained by Figure7 at 5 ns the output should be determined. The time required for this channel has 3.27 ms.

Table I shows the CPU and ELAPSED time required for channel model. Initial condition of CPU has 1.99 ms and usage is 1.055 ms. The time accumulated for CPU has 253.96 ms and 940.988 ms for usage time. The memory should be used as 33.4 Mbytes.

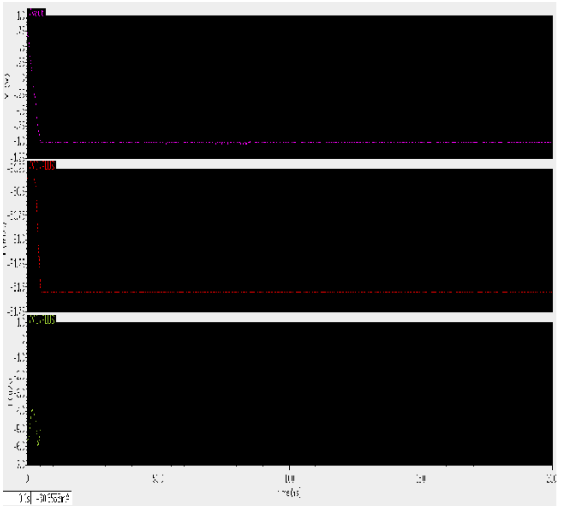

Fig7: Simulation of Channel Output

Table 1: CPU time and ELAPSED time required for channel model of transient analysis

CONDITION	CPU TIME	ELAPSED TIME
Initial condition Solution time	1.999 ms	1.055 ms
Intrinsic tran analysis time	7.999 ms	8.13508 ms
Total time required for tran analysis	12.997 ms	17.987 ms
Time accumulated	253.96 ns	940.988 ns

The conditions of values and changing the input parameters and modify the output and the time was analyzed for different conditions of transient and DC analysis.

Table II gives the DC analysis of CPU and ELAPSED time. The total time required for CPU has 821.875 ms and usage time has 850.942 ms. The time accumulated for 1.02684 s for CPU and 1.67693 s for usage time. The peak memory used as 29.8 Mbytes

Table 2: CPU time and ELAPSED time required for channel model of DC analysis

CONDITION	CPU TIME	ELAPSED TIME
Total time required for DC analysis	821.875 ms	850.942 ms
Time accumulated	1.02684 s	1.67693 s

Figure8 gives the Schematic diagram of transmitter block. In this clock and reset are input to the block and generate patterns of vector _data and acknowledgments are output to the transmitter block. The signals are converted to patterns and vector has 8 bit data and data has 12 bit data it should be multiplied and get 192 patterns of vector.

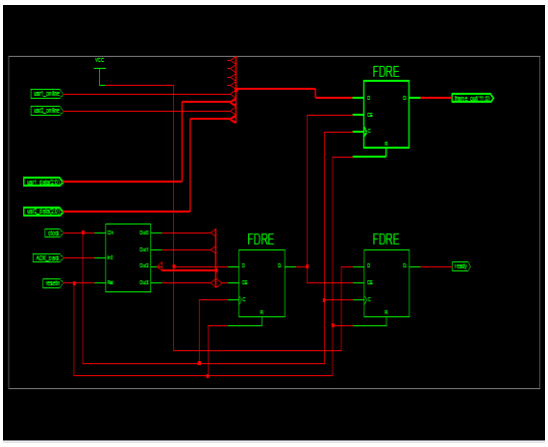

Fig8: Schematic diagram of transmitter

Next the inputs are given to test bench waveform. In Xilinx the inputs are given to each vectors and clock sign5al should be changed as well as input of the other data was modified.

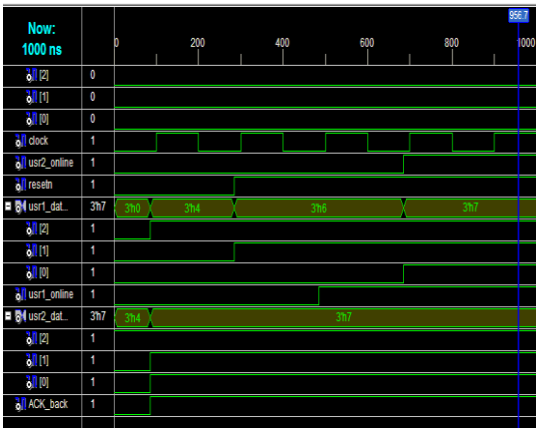

Fig9: Output waveform of transmitter block

Figure9 shows the output waveform of the transmitter block. In this transmitter the inputs are vector and data are multiplied and generate convert vector and convert data and the results are stored in patterns of the transmitter block.

CONCLUSIONS

In, this paper by designing a MC-DS-CDMA system in virtuoso environment using cadence the good accuracy of the design is obtained and several different parameters can be determined. Such as, the memory required, execution steps required, CPU time and elapsed time required The performance of MC-DS-CDMA transmitter block was analyzed using Analog design. From this result we can conclude that the information to be encoded and transmit over the channel and decode the original information .It can be used for the mobile application. This work can be further enhanced by undergoing the process of implementation. To design a new algorithm for Concatenated code in Serial and parallel code. To create code for MC-DS-CDMA blocks using various description Languages like Verilog and VHDL. Create a new technique to reduce power consumption of overall system.

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