

A REVIEW ON GLITCH REDUCTION TECHNIQUES

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Abstract

This paper presents different techniques for reducing glitch power in digital circuits. The aim of this study is to minimize glitch power as glitch power comes under dynamic power, so that power dissipation will reduce up to some extent in digital circuits. Warren Shum et.al [2011] work shows glitch power in FPGA's varies from 4 % to 73 % of total dynamic power having an average of 22.6 %. Warren Shum et.al [2011] and J. Lamoureux et.al [2008] motivates us to reduce glitch power in digital circuits as well as FPGA's. Different techniques are available for reducing glitch power like gate sizing, gate freezing, multiple threshold transistors, hazard filtering, balancing path delay, by reducing switching activity etc.

Keywords: Glitch, Power dissipation, Gate sizing, Gate freezing, multiple threshold transistor, Hazard filtering, balancing path delay and switching activity.

1. INTRODUCTION

Un-necessary signal transitions that do not have any functionality are known as glitches [3]. Nowadays, power dissipation is a very burning topic, everybody in search of how to minimize power dissipation in daily use devices like laptops, mobile phones, mp3 players etc, particularly for handy devices because most of the gadgets today are battery operated that requires low power consumption. Total power dissipation consists of mainly dynamic power dissipation and static power dissipation, further these dynamic and static power dissipation divided in to others like leakage power dissipation, switching power dissipation and short circuit power dissipation as shown in equation (1) and (2).

$$P_{\text{Total}} = P_{\text{static}} + P_{\text{dynamic}} \quad (1)$$

$$P_{\text{Total}} = P_{\text{Switching}} + P_{\text{Short-Circuit}} + P_{\text{leakage}} \quad (2)$$

Dynamic power dissipation is a major source of leakage power, that is directly proportional to the number of signal transitions (0 – 1 and 1 – 0) in a digital circuit [4]. Signal transitions are of two types: functional transition and a glitch. According to reference [4] glitch power dissipation is 20 % to 70 % of total power dissipation. By varying gate delays and path delays in the circuit glitches can be reduced to some extent. Glitches are the source of un-necessary power dissipation, misalignment of signal transitions and gate delays are the major sources for glitches in digital circuits [5]. Switching power dissipation ($P_{\text{Switching}}$) is directly proportional to switching activity (α), load capacitance (C_{load}), supply voltage (V_{dd}) and clock frequency (f_{clk}) as shown in equation (3).

$$P_{\text{Switching}} = \alpha \cdot C_{\text{load}} \cdot V_{\text{dd}}^2 \cdot f_{\text{clk}} \quad (3)$$

Switching activity means charging and discharging of load capacitor also we can say transition from low to high level (0 – 1) and high to low level (1 – 0). As glitches are dependent on signal transitions so more switching activity will result in more glitches in a digital circuit and more power dissipation will be there [6]. According to equation (3) switching power dissipation can be controlled by controlling switching factor, voltage scaling etc.

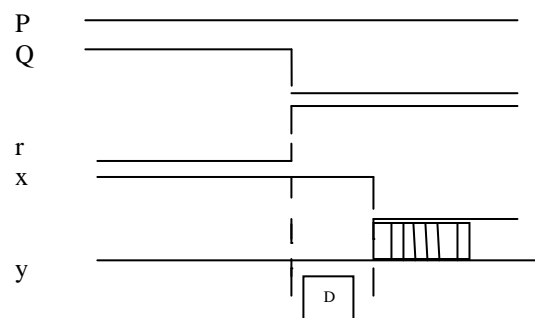


Fig 1 Graph showing glitch in the output of 3 input digital circuit.

The graph shows glitch in the output as in Fig. 1 where p, q, r are the inputs, x and y are the outputs and 'D' is delay that generates glitch in the circuit [6]. Here in this paper different techniques are discussed for minimization of glitches and total power consumption in the circuit like gate sizing, balancing path delays, hazard filtering, by reducing switching activity, multiple threshold transistors.

2. TECHNIQUES FOR GLITCH REDUCTION

2.1 Gate Sizing

Gate sizing affects glitch transitions but does not affect functional transitions. A glitch may generate after resizing of a gate but the next gate in that circuit does not allow it to propagate throughout the circuit. Generation of glitches during resizing may result in a bad solution. To come out of these type situations “simulated annealing” will be done, which is too much costlier. So keeping in view all these things, Masanori Hashimoto et.al has developed an analytic algorithm which is not too much costlier that takes out from a bad situation also. Following there are three steps for performing an analytic algorithm these are :

- Step I: Calculate the sensitivity of the objective function of each gate by gate resizing.
- Step II: According to the calculated sensitivity select and resize the gates. The number of resized gates is at most Max_change. Optimization procedure stops if there are no gates which has the sensitivity of reducing object function.
- Step III : Optimization procedure stops if iteration count comes out more than a pre-defined value. Max_iteration reduces Max_change by a factor of Reduce_rate and go back to Step I.

Calculate the sensitivity of the objective function both for sizing up and sizing down operations. According to the sensitivity resize the Max_change gates from highest, if number of gates with positive sensitivity is more than Max_change. Resize all the gates if number of gates with positive sensitivity is less. Resizing of gates in the circuit is disruption to the circuit. As the number of Max_change is reduced in the iteration disruption will be reduced. As in Step I. Max_change value is large so number of gates that was resized will also large and more disruption will be there. But when process increases in steps Max_change parameter will reduce at the rate of Reduce_rate and disruption will also reduce. At the last step, Max_change becomes too small and this algorithm behaves like a self-indulgent algorithm. Good solution can be founded out with the help of disruption and self-indulgent. Changing all the three parameter (Max_change, Max_iteration and Reduce_rate) values we can reduce disruption and increase speed of the circuit [7].

2.2 Gate Freezing

This method minimizes power dissipation in CMOS circuit by eliminating glitch. According to extracted information from gate net list, more glitchfull and high power dissipating gates will be selected and replaced by a modified library cell called ‘F-gate’ with a control signal (CS) [8] as shown in Fig. 1, where Vdd is supply voltage, I is input, O is output CS is control signal to n-type library cell and Gnd is ground.

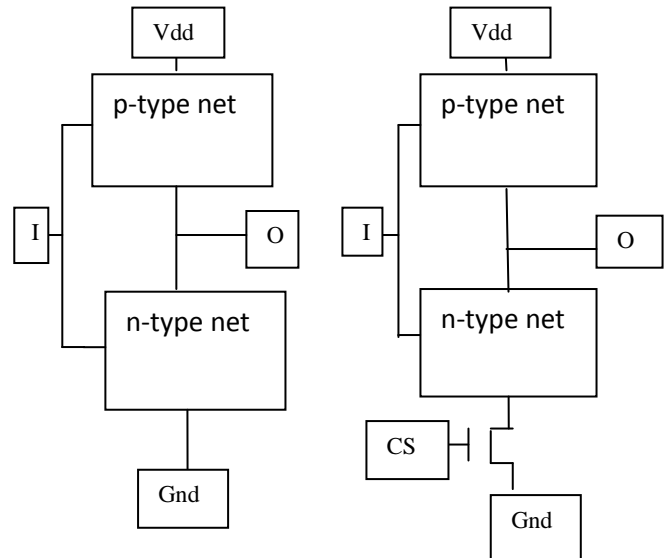


Fig 2 CMOS inverter and CMOS inverter with library cell

This gate is controlled in order to “freeze” the cell’s (n-type transistor) output for reducing the amount of glitch from the circuit. Basic CMOS is little bit different as compared with CMOS library cell structure, only a library cell (n-type transistor) is connected in series with n-type network of CMOS as shown in Fig. 2. The gate input of this n-type cell is driven by control signal (CS). This method transforms some of the gates that are more glitchfull into modified devices that are able to filter out unnecessary output transitions when a control signal (CS) is activated. With the help of topological timing analysis the information of arrival time, required time and slack time at each stage will be calculated. Event driven simulation can be performed to get all the activity information of glitch. According to the results of topological timing and event driven simulation, we can easily select more glitchfull and high fanout gates. This method puts the control signal (CS) to logic ‘0’ until the elimination of glitch of the selected gates. When the control signal of n-type transistor is high or at logic ‘1’ all gates operate in normal mode. But when CS is at logic ‘0’, n-type transistor is disconnected from the ground. So that CMOS can never be discharged to logic ‘0’ [8]

2.3 By Reducing Switching Activity

As mentioned in introduction that glitches depend on switching factor (transitions), signal transitions are of two types: functional and glitch transition. Switching power is directly proportional to switching activity (α) as shown in equation (3). So, more transitions will result in more glitches and more power dissipation will be there. Here in this section an example of 3 bit counter is explained that how to reduce glitches and finally less power dissipation. A state diagram of 3-bit counter using binary code and grey code was drawn as shown in Fig. 3 and Fig. 4 respectively.

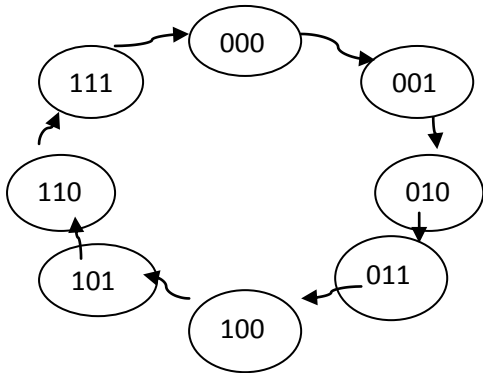


Fig 3 State diagram for 3-bit counter using binary code

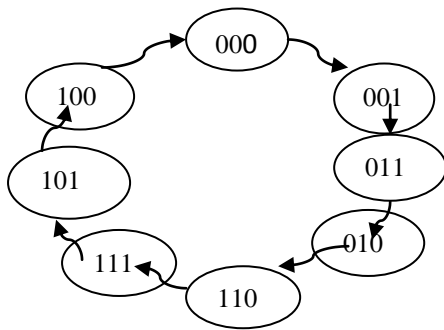


Fig 4 State diagram for 3-bit counter using grey code

Number of transitions from '000 to 001' is 1, '001 to 010' is 2 etc was calculated for both binary and grey code 3 bit counter. Total number of transitions in binary code 3 bit counter was 14 and in case of grey code 3 bit counter it was only 8. So, number of transitions per cycle is $14/8 = 7/2$ and $8/8 = 1$ in binary and grey code 3 bit counter respectively. As number of transitions per cycle is 1 in case of grey code 3 bit counter, so glitches will definitely be reduced and low power dissipation.

2.4 Multiple Threshold Transistor

This is a new technique for reducing glitch and power dissipation in digital circuits. As delay of each gate is a function of threshold voltage (V_{th}), gates that are in non critical paths were selected and their threshold voltages (V_{th}) rose manually, then the propagation delays along different paths can be balanced so that unnecessary transition will be minimized. By rising threshold voltage (V_{th}) of the transistor that are in non critical path will also minimize leakage current in the same path. Applying this method to the digital circuits will not affect the performance of the circuit because performance is calculated from the critical paths. So this technique is a new efficient technique for minimizing glitch in digital circuits that leads to low power dissipation [6].

2.5 Hazard Filtering and Balanced Path Delay

Hazard in digital circuits is unnecessary transitions as in case of glitch due to gate propagation delay in that circuit. A circuit was taken with equal gate propagation delays of 2 unit each as shown in Fig. 5.

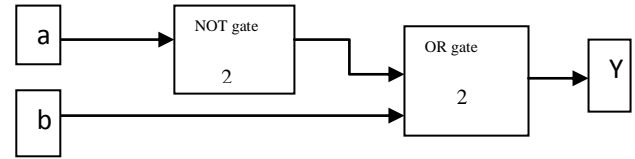


Fig 5 Original circuit with glitch output

The output (Y) of this circuit was glitchy in nature due to different path delays of OR gate inputs. For removing this condition balanced path delay technique was used. Let's take a look of the same circuit after applying balanced path delay technique (in this buffers were inserted) as shown in Fig. 6.

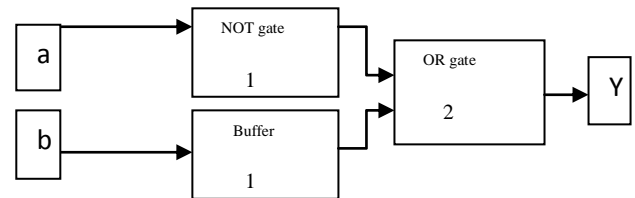


Fig 6 After applying balanced path delay technique

Now output of the circuit came out non-glitchy as path delays of OR gate inputs were balanced. After this Hazard filtering technique was applied for removal of glitch from the circuit. In this technique buffer insertion was not used, gate propagation delays were adjusted as shown in Fig. 7.

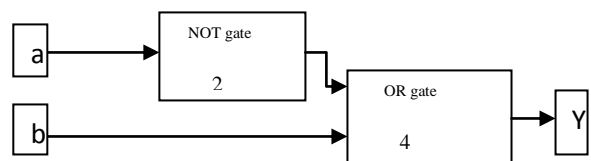


Fig 7 After applying hazard filtering technique

In this we just increased the gate propagation delay of the final OR gate to '4'. So that all the path delays will be balanced till the OR gate operation. Hazard filtering technique is better than balanced path delay technique as balanced path delay technique is more power consuming than hazard filtering technique due to buffer insertion in the circuit in case of balanced path delay technique [9].

CONCLUSIONS

As we discussed different types of techniques for glitch reduction in digital circuits. Here some conclusions were made according to the references. Masanori Hashimoto et.al work shows gate sizing technique not only minimizes amount of capacitive load, short-circuit current, but it also minimizes glitch transitions. Glitch transitions were reduced up to 38.2 % on an average with total reduction by 12.8 % and 7.4 % reduction in total power dissipation. Glitch power consumption on an average improved by 65.64 % and total power consumption improved on an average by 31.03 % with the help of gate freezing technique [8]. Zhanping Chen et.al used three threshold transistors for minimizing glitch power, and using this technique reduced the glitch power by 30 % approximately. In case of hazard filtering speed of the circuit became slow as per the study done but circuit consumes less power as it is reverse in case of balanced path delay technique. So hazard filtering is better technique than balanced path delay technique.

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BIOGRAPHIES



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