DESIGN OF ALL DIGITAL PHASE LOCKED LOOP (D-PLL) WITH FAST ACQUISITION TIME

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Abstract

A Digital PLL is designed with improved acquisition time and power efficiency. The implemented D-PLL can operate from 6.54MHz to 105MHz with a power dissipation of is 7.763µW (at 210MHz) with 1.2V supply voltage. The D-PLL is synthesized using cadence RTL compiler in 45nm CMOS process technology.

Keywords: Digital PLL, Digital Phase/Frequency detector, NCO, Divide by N counter.

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1. INTRODUCTION

Phase locked loops are widely used in frequency synthesis applications [2], [4]. For many portable applications the acquisition time of PLL is very important so the design of PLLs with minimum acquisition time is the primary goal of this work .A Phase Locked Loop (PLL) is a feedback system that compares the output phase with the input phase to produce an output signal that has the same phase as that of an input signal. PLL's are found in many applications such as reference generation, frequency synthesis, frequency multiplication, FM demodulation etc. As the frequency of operation increases, the need of generating signals that are in phase lock with input (i.e. fast varying signals) is becoming a problem. There are two types of PLL's 1.Analog PLL 2.Digital PLL. Traditional PLL's are Analog PLL's are shown in fig.1

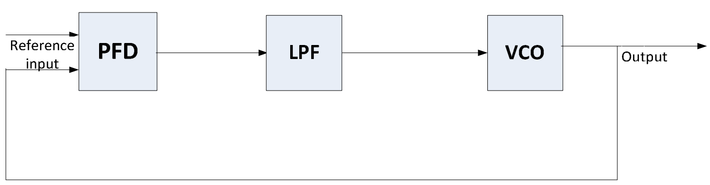

Fig.1 Block diagram of Analog PLL

It uses phase detector to compare the input phase with the output phase. Loop filter is used to reduce the ripples on the control voltage of VCO. VCO is used to adjust the output frequency such that the loop is locked and the output signal is the replica of the input signal.Analog PLLs occupy larger chip area due to the use of capacitors in feed forward path. It has some other disadvantages such as sensitive to noise and difficulty in converting to different processes and etc. Whereas D-PLLs are compact and high immune to noise. Moreover D-PLLs are easily programmable (i.e. easy process conversion).

2. D-PLL ARCHITECTURE

The block diagram representation of a D-PLL is shown in fig.2. The below architecture is simple and easy to implement.

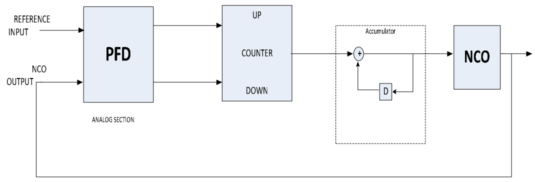

Fig.2 Block diagram of D-PLL

The D-PLL architecture shown above has four major blocks, namely the phase/frequency detector (PFD), the time to digital converter (TDC), the accumulator and the numerically control oscillator (NCO).The NCO is implemented by using frequency divider circuit. The PFD detects the phase or frequency difference between the reference clock and output clock. The output of the PFD is given to TDC which is continuous in time. The time to digital converter generates a count value which is proportional to the phase error. The average value (DC value) of the PFD is accumulated by the accumulator block. The accumulated valve determines the control word for the NCO to oscillate with an appropriate frequency.

Analysis of Individual Blocks

A. Phase Detector:

The Phase detector (PD) is a circuit that compares the phase difference between the two input signals. It generates an output signal whose average value is linearly proportional to the phase difference between the two input signals. There are number of ways in which a Phase Detector can be realized, but we mostly consider two types. They are 1) XOR-gate 2) PFD.

a) XOR-Gate Phase Detector:

The XOR-gate produces an output when both the inputs are unequal, otherwise zero. The XOR gate Produces output both at the rising edge and falling edge of a cycle. The below equation gives the input-output relationship of an XOR- gate Phase Detector

$$\overline{V_{out}} = \frac{1}{2\pi}\left[\int_0^{\Delta\emptyset} V_0 d\emptyset + \int_{\pi}^{\pi+\Delta\emptyset} V_0 d\emptyset\right]$$

$$= \frac{1}{2\pi}[V_0 d\emptyset + V_0 d\emptyset]$$

$$= \frac{2V_0\Delta\emptyset}{2\pi} = \frac{V_0}{\pi}\Delta\emptyset$$

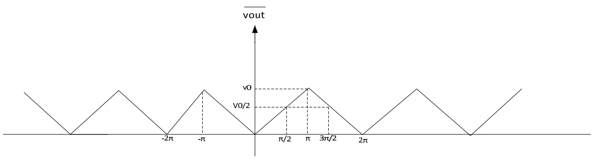

Fig.3 I/O Characteristics of XOR-Gate Phase Detector.

As it can be seen from the above characteristics, the problem of XOR-gate Phase Detector is its linearity range is limited to π. When the phase difference is greater than π then its average output value decreases. So we go for flip- flop base phase Detector or Phase Frequency Detector.

b) *Phase Frequency Detector(PFD):*

The circuit shown in fig.4 can serve as both phase/frequency detectors. It has three states, initially both and equal to zero. If input A leads input B, first goes high at the rising edge of input A (since is connected to logic 1), then goes high at the rising of input B (since is also connected to logic 1), causing the output of the NAND gate to go to low, thereby resetting both and .Similarly if input B leads input A then goes high first edge.

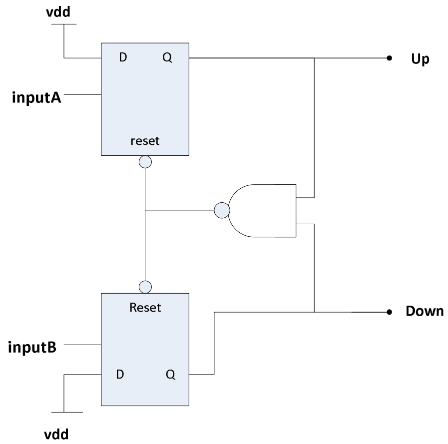

Fig.4 Block diagram of PFD

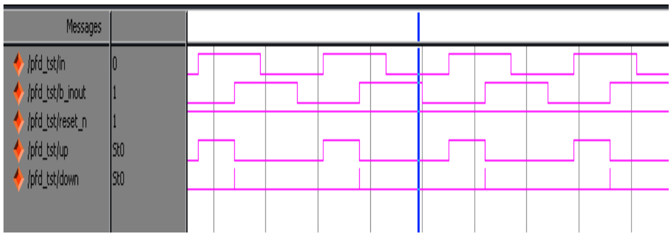

Fig.5 Output waveforms of PFD

The circuit consists of two positive edge triggered, negative edge resettable D-flip-flop having tied their inputs to logical 1.The input's of interest serves as a clock to flip-flop. The input's of interest serves as a clock to flip-flop. The input output characteristics of the phase frequency detector is shown below:

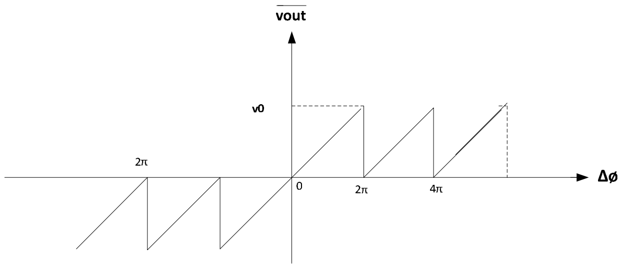

Fig.6 Input-Output characteristics of PFD

From fig.6 it is clear that the main advantage of Phase Frequency Detector is that it's improved linearity range and the ability to act as a frequency detector as well.

B. Integrator:

The integrator block consists of time to digital converter plus discrete time accumulator (1 tap IIR filter) to provide a fixed value to the NCO

a) Time to digital converter:

The time to digital converter block is used to convert the output of the Phase Frequency Detector which is continuous into a digital number. The time to digital conversion can be achieved simply by using a counter which is capable of counting up and down. The following analysis has shown that the output count value is proportional to the input Phase Difference.

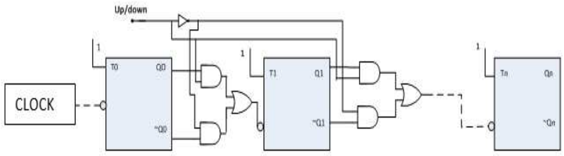

Fig.7. Time to Digital Converter (TDC) implemented with Counters.

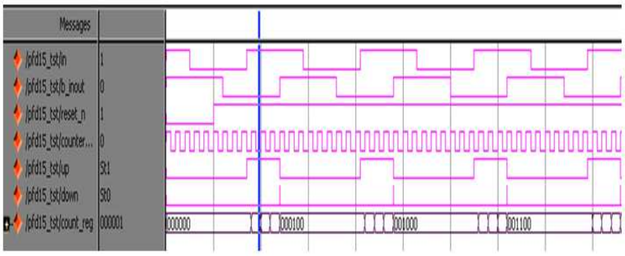

Fig.8. Output Waveforms of Time to Digital Converter

Let C= Counter Output;

C (t) = time varying state of Up/Down counter.

Δt=Counter clock period.

T=time period of input or phase detector cycle period.

$$C = C_0 + \sum_{i=1}^{N1} c(t)\,.\Delta t \text{ ----- (1)}$$

If Δt is very small i.e. if $\Delta t \rightarrow 0$ then $\sum$ becomes integration.

$$C = C_0 + \int_0^{N1} c(t)\,.\,dt \text{------- (2)}$$

If there are N_1 cycles in T seconds then

$$f_1 = \frac{1}{T_1} = \frac{N_1}{T} \text{ --------- (3)}$$

Where f_1=counter clock frequency.

$$N_1 = f_1.T$$

$$C = C_0 + \int_0^{f\,1.T} c(t).\,dt = C_0 + \int_0^{f1.\Delta\emptyset} 1.\,dt = C_0 + f_1.\Delta\emptyset \text{ ------ (4)}$$

From equation (4) it is clear that the output count value C is proportional to the input phase difference $\Delta\emptyset$.

b) Accumulator (Discrete time integrator):

The accumulator block is used to provide a constant number (control_ word) to the Number Control Oscillator (NCO). The accumulator block is analogous to the LPF (integrator) in analog PLL. The accumulator block accumulates the phase difference between the reference clock and the output clock to provide a constant value to the NCO. Otherwise the input to the NCO varies periodically with time which results in varying frequency at the output thus phase locking cannot be achieved.

C. Number Control Oscillator (NCO):

The Output frequency of the NCO is numerically controlled by using a binary word instead of voltage. That is the NCO generates an output signal whose frequency is proportional to the input control word (binary format). There are many ways to implement NCO block but the simplest way to implement NCO is counter based approach. The NCO consists of counter capable of dividing the input clock based on its control word. The applicability of this device as NCO is explained below.

$$F_{out} = \frac{f_2}{2^n} * Controlword$$
$$= k * Control\,word \text{ ----- (1)}$$

Where k= Resolution $= \frac{f_2}{2^n}$, *n= No. of bits in counter.*

The resolution of NCO increases by increasing the number of bits. The higher the control word, higher the frequency and vice-versa.

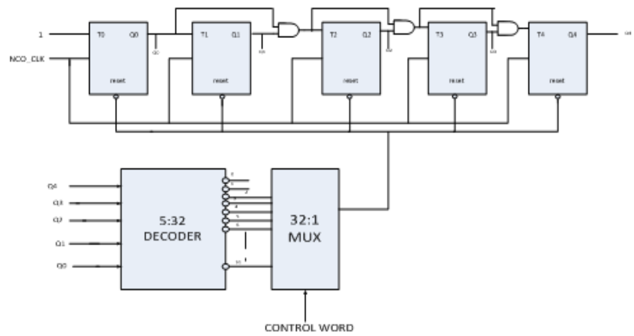

Fig.9 Internal block diagram of NCO

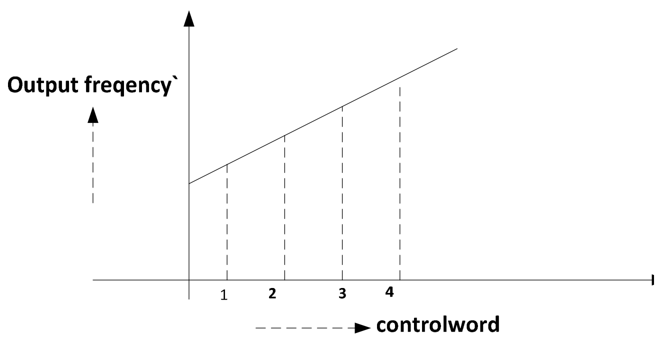

Fig.10 Input- output characteristics of NCO

From equation (1), it is clear that the NCO can be implemented using counter, whose output frequency is based on the Control word. The maximum input frequency that can be locked depends on the NCO resolution

($k=\frac{f_2}{2^n}$).The counter based NCO frequency range is $\frac{f_2}{2} > f > \frac{f_2}{2^n}$.

3. SIMULATION RESULTS:

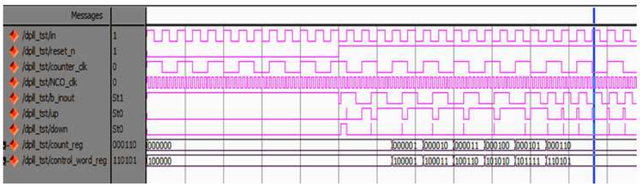

Fig.11 Output waveforms of PLL at 210MHz

Fig .11 shows the Output waveforms of the PLL where the reference clock is 52.35MHz. The D-PLL is synthesized using cadence RTL compiler in 45nm CMOS process. The D-PLL is implemented with following specifications.

Specifications:

1. Maximum NCO frequency = 209.42 MHz
2. Free running frequency of NCO = 130.8MHz.
3. NCO resolution = $\frac{f_2}{2^n}$= 6.54MHz; n=5 bit.
4. Input Frequency = 7MHz.

From the comparison table it is clear that power dissipation of the proposed D-PLL is minimal compared to that of All Digital cell based PLL [1], Analog PLL [2], Semi-Digital PLL [3]. The acquisition time of proposed D-PLL is less than Digital cell based PLL[1] and analog PLL[2] i.e. proposed D-PLL is faster than the other two PLLs proposed in [1],[2].

Table 1.Performance Comparison

Performance Parameter	Our DPLL	[1]	[2]	[3]
Process	0.045µm	0.35µm CMOS	0.25µm CMOS	0.60µm CMOS
Approach	All digital	All-digital cell based	Analog	Semi-digital
Power dissipation	7.763µW (@210MHz)	100mW(@500MHz)	25mW	105mW(@400MHz)
Minimum Frequency	6.54MHz	45MHz	8.5MHz	300MHz
Maximum Frequency	105MHz	510MHz	660MHz	800MHz
Supply voltage	1.2v	3.3v	1.9v	3.3v
Max. acquisition time	<18 cycles	<46 cycles	<720 cycles	<16 cycles

4. CONCLUSION:

The D-PLL is implemented with standard cells in a 0.045µm technology and can operate from 6.54MHz to 105MHz. The presented D-PLL architecture is simple and easy to implement. The acquisition time is 18 cycles.

REFERENCES:

[1] H.-T.Ahm and D.J.Allstot,"A low-jitter 1.9-V CMOS PLL for ultraSPARC microprocessor applications,"IEEE J.Solid-States Circuits, vol.35,pp.450-454,May 1999.

[2] I.Hwang, S.Lee, S.Lee and S.Kim,"A digitally controlled phase locked loop with fast locking scheme for clock synthesis applications,"in IEEE Int.Solid-State circuits Conf.Dig.Tech.Papers, Feb.2000, pp.168-169.

[3] A. Young, M. F. Mar, and B. Bhushan, "A 0.35-m CMOS 3-880-MHz PLL N/2 clock multiplier and distribution network with low jitter for microprocessors," in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, Feb. 1997, pp. 330–331.

[4] Ching-Che Chung and Chen-Yi Lee,"An All-Digital Phase-Locked Loop for High-Speed Clock Generation," IEEE JOURNAL OF SOLID STAES CIRCUITS, VOL.38, NO.2, FEBRUARY 2013.

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