FAULT MODEL ANALYSIS BY PARASITIC EXTRACTION METHOD FOR EMBEDDED SRAM

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Abstract

Fault analysis plays a significant role in developing detailed fault models for subsequent diagnostics and debugging of a semiconductor memory product. Existing fault models were analyzed in terms of well known March algorithms. Such analysis is able to give information only on either detection of fault or correction. But they are failing to give information based on various constraints such as dynamic power analysis, propagation delay analysis, and the bit line capacitance influence while reading or writing the data. Scale down in technology causes changes in parasitic effects, which may cause additional source of faulty behavior. Hence we suggest an analysis which includes majority of these constraints with the help of layout based fault model. Finally different parametric values are compared for faulty and fault free SRAM cell. We found that although some of the defects can be mapped to existing fault models, there are many defects that result in undefined fault models.

Keywords: *fault models, March algorithms, dynamic power analysis, propagation delay analysis, bit line capacitance, layout based fault model, undefined fault models.*

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1. INTRODUCTION

The growth in the technology depends on many facts, one fact is human thrust towards innovation and the other fact is force by existing technology towards upgraded technology to fulfill the drawbacks in the existing technology. This leads to up gradation from VLSI technology to ULSI which results in reduction in the size and the cost but also increases the complexity of the circuits. This has brought significant improvements in performance. In spite of the advantages such as better performance with low cost, significant problems which may encounter the effective use and growth of future VLSI technology. Also the circuit testing becomes more complex as scale of integration increases.

Recent developments in system-on chip technology demands large embedded memory to incorporate into a chip. Circuit density increases with levels of integration. Hence efficient testing schemes are needed that assure very high fault coverage while minimizing test costs and chip area overhead. As the complexity of circuits continues to increase, high fault coverage of several types of fault models become more difficult to achieve. The usage of SRAM is continuously increasing in system-on-chip (SOC) designs. Process technology scaling has contributed remarkably in improving the performance of SOC in terms of area and density. As the feature size of components shrinks the sensitivity to faults increases while the faults become more complex. Furthermore, test time grows at least linearly as the number of storage elements per chip increases [1, 2, and 3].

The SRAM cell typically utilizes the minimum sized transistor in order to realize a high density [4]. Technology scaling leads to increased intra die variations and its impact is more pronounced on the SRAM cells. As a result SRAM scaling has become extremely difficult in the advanced technology nodes (e.g., 65, 40, or 32 nm LP CMOS technology). The lowest operational VDD (VDDmin) for embedded memories (SRAM) is limited by either read (cell stability) or write ability. SRAM bit cell functional parameter degradation due to increasing variability and decreasing power supply is of utmost concern. The random threshold variations in sub nanometer technologies have resulted in serious yield issues for realizing low VDD READ/WRITE operations with a 6T SRAM cell. The area of an SRAM cell is very important because the cell area contributes significantly to the silicon area. For instance, SRAM L1 caches occupy a significant portion of many designs. The minimum sized 6T cell in 65 nm occupies 0.4 µm2 (Utsumi et al. 2005), in the 40 nm 0.33 µm2 (Yabuuchi et al. 2007), and in the 32 nm 0.124 µm2 (Chang et al. 2005).As the SRAM cell is scaled, it is difficult to ensure cell stability. For low VDD values, the signal level reduces because of the impact of Vt variations. SRAM cell design can be optimized to minimize the impact of Vt variation on signal read. The SRAM cell beta ratio is defined as the (W/L) of NMOS pull down transistors of inverter to the PMOS pull up transistor.

The reference number should be shown in square bracket [1]. However the authors name can be used along with the reference number in the running text. The order of reference in the running text should match with the list of references at the end of the paper.
Eg1: As per Kong, the density of X increases with Y [9].
Eg 2: It is reported that X increase with Y [45].

1.1 Power Dissipation Concepts

1) Dynamic Power Dissipation:

The main elements in the power dissipation are the switching activity of each node, the supply voltage, the voltage swing on each node, the capacitance at each node and the clock frequency.

$$P=\alpha.f.C.VDD.\Delta V$$

Where α is the switching activity, C is capacitance, f is clock frequency, and ΔVis the output voltage swing.

2) Static Power Dissipation:

The reason behind the static power dissipation to occur in the circuit is when a node that does not achieve full voltage swing used to drive another circuit. Another reason is leakage currents when the gates operating in the idle mode. CMOS gates consumes a certain amount of power when leakage current passing through the transistors. As the level of doping has to be increased due to transistors shrink in the size causes leakage currents to become larger. This effect is more pronounced when millions of transistors are involved.

3) Reasons of Power Dissipation during Testing:

The main reasons for the power dissipation during testing are so many. Few among them are discussed here. More the complexity of the circuit leads to more test time. Hence to save test time, it requires to partition the circuits so that test stimuli can be applied in parallel to all the circuits at a time. But partition of the circuits may leads to high power dissipation. Due to lack of at-speed equipments, delay is introduced in the circuit during testing which also dissipate power. In the testing mode, the correlation between the consecutive patterns is small which causes large switching and hence increases the dynamic power. In normal mode, only a small part of the SOC works but in the test mode all blocks of the SOC remain engaged by applying the large number of test patterns one after the other. Hence, test mode requires more power than normal mode and responsible for increasing chip temperature. Circuit power dissipation in test mode is much higher than the power dissipation in function mode [5]. Some algorithms such as March LR produce a high circuit switching activity, which is the major cause of heat dissipation. Test efficiency correlates with toggle rate, correlation between successive functional inputs may be significant, and however, for test patterns it is generally kept low.

Generally faults can be divided in to time invariant (permanent) and time varying categories. A permanent fault is a fault which manifests a faulty behavior regardless of any operating conditions. There are two types of non-permanent faults; they are Transient fault and intermittent fault. Transient fault is a fault which is time dependent, caused by environmental conditions. Intermittent faults are caused by non-environmental conditions such as Loose connections, Deteriorating or aging components, Critical Timing, Resistance and capacitance variation, Physical irregularities, noise (noise disturbs signals in the system). Many fault models have emerged for permanent and transient faults which uses March algorithms. But such fault models are not suitable for the study of intermittent faults. And also they are failing to give information based on various constraints such as dynamic power analysis, propagation delay analysis, and the bit line capacitance/resistance variation while reading/writing the data.

By taking all the above said constraints such as read /write latency and power dissipation as measures, the analysis is made on SRAM single cell with and without fault using their layout simulations. In this analysis various parameters such as critical path delay, power dissipation over a range of capacitances, node values in terms of total capacitance, resistance, and dynamic power dissipation, propagation delay were observed and compared. These are all performance measures to consider while optimizing the yield of SRAM. Section II discuss about the impact of bit line capacitances on read and write operations in SRAM cell, Section III discuss about parametric analysis which deals with propagation delay, dynamic power dissipation, and different node values. Section IV discusses results and comparisons and Section V gives conclusions

2. BIT LINE CAPACITANCE AND THE IMPACT ON READ/WRITE OPERATIONS

The generic SRAM cell as shown below turns out to be quite similar to the static SR latch. It requires 6 transistors per bit. At first, it seems like the margins in such a memory cell should be good, since it contains two CMOS inverters, which we know have large margins. However, the problems are associated with those access devices connected to the cell. When cell is not accessed, it has great margins; when access devices are on, they act like load devices. Capacitance on bit lines is large enough to act like a voltage source. Read operation is as shown below in fig.1.

In this Read Operation assume first that node Q is in the "1" state, we further assume that both bit line are pre charged to VDD, 2.5V, before the read operation is initiated. The read cycle is started by asserting the word line, enabling both

transistors M5 and M 6. During a correct read operation, the values stored in Q and !Q are transferred to the bit lines by leaving BL at its pre charge value and by discharge !BL through M1 – M5 . A careful sizing of the transistors is necessary to avoid accidentally writing a "1" into the cell. This type of malfunction is called "read upset" [6].

Initially, upon the rise of the WL, the intermediate node between these two NMOS transistors M1 & M5, Q, is pulled up toward the pre charge value BL. This voltage rise of Q must stay low enough not to switch inverter of M3 and M4, which will flip the cell. It is necessary to keep the resistance of transistor M5 large enough to prevent this from happening. The boundary constraints on the device sizes can be derived by solving the current equation at the maximum allowed value of the voltage ripple ΔV where ΔV is noise margin of the inverter. Since both M5 and M1 are in velocity saturation region, by equating their current equations the cell ratios can be obtained and is as follows:

$$k_n'(\frac{W}{l})_{m5}[(v_{dd}-\Delta v-v_{t,0})v_{dsat,n}-\frac{v_{dsat,n}^2}{2}]=k_n'(\frac{W}{l})_{m1}[(v_{dd}-v_{t,0})v_{dsat,n}-\frac{v_{dsat,n}^2}{2}]$$

The cell ratio is (w/l) m1 to (w/l) m5. For large memory arrays, it is desirable to keep the cell size minimal while maintaining read stability. If the transistor m1 is minimum sized, the access pass transistor m5 has to be made weaker by increasing its length. This is undesirable, because it adds to the load of the bit line. The total BL capacitance (Ct) is divided into three components: internal coupling capacitance due to complementary bit line !BL (Cbi), external coupling capacitance due to a neighboring bit line BL (Cbx) and an inherent BL capacitance to ground (Cg) composed of coupling to all other parts of the memory (cells, WLs, substrate, etc)[7]. This is expressed as:

$$Ct=Cbi+Cbx+Cg$$

The exact values of these capacitances depend on the layout of the memory and its manufacturing technology. In general, the value of Cg accounts for a large portion of Ct. In literature, reported Cg/Ct ratios range from 40% to over 90% [8]. On the other hand, due to the symmetry of the layout implementation of the bit lines BL and !BLs, the values of Cbi and Cbx are rather close to each other, and therefore we consider them to be equal (Cbi=Cbx=Cb) such that: Ct≈2Cb+Cg.

In general SRAM deals with read and write operation. But read operations are more sensitive to the impact of coupling than write operations. During a read operation, the WL accesses the cell and connects it to the pre-charged BLs. Based on the value stored in the cell, a voltage difference develops on the BLs that the sense amplifier subsequently attempts to detect. The presence of Cb causes neighboring BLs to influence the voltage development during a read. If we assume that a defective BL is totally floating, while the neighboring BL develops a voltage V, then the amount of coupling voltage (ΔV) induced on the floating BL can be expressed as:

Because of excessive bit line BL the common faults may occur in the memory are coupling fault (CFs), Bit line voltage imbalance fault (PSF), Single ended bit-line voltage shift (PSF). The excessiveness in BL occurs when there is coupling between bit line BL and word line WL. Hence one can identify the type of fault by careful study of bit-line capacitance analysis.

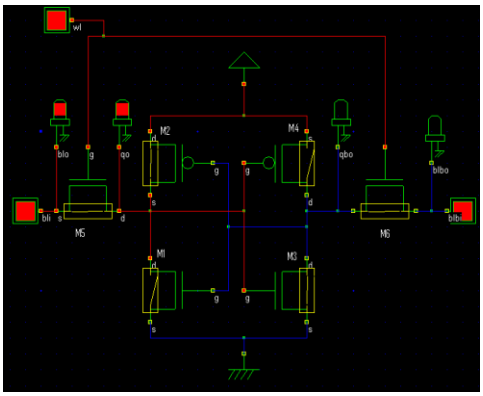

Fig -1: SRAM cell with Read operation

3. PARAMETRIC ANALYSIS

3.1 Propagation Delay:

There are several causes for delay in the 6T SRAM. The first is due to the time it takes the input data to reach bit-lines, which depends on the switching time for both the external writing circuitry and the bit-lines. The others arise from the W/R word-line switching and N1 and N2 turning on, followed by the stored voltages in the memory latch being overwritten. All of these are directly related to the amount of capacitance on the lines or nodes being charged or discharged. When there are process variations within a single memory cell – scenarios more likely to occur at 20nm – read, write, access, or hold failures can occur [9].

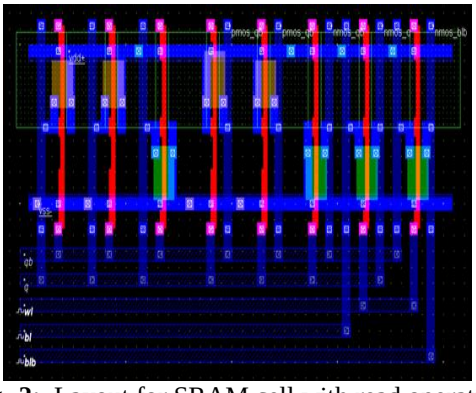

Fig -2: Layout for SRAM cell with read operation

The propagation delay is one of the key parameter which affects the performance of SRAM. Increase in rise time will show impact on performance, whereas increase in fall time show direct impact on memory functionality. If fall time increases, pass transistor active period increases (read operation). If the bit line over-discharge, the memory content over-charge during the read operation. If the over-discharge is present this increases the dynamic power dissipation of bit lines, which in turn causes the cell content to flip if the over-discharge period is large.

3.2 Power Dissipation:

Technology variation causes process parameters variations such as channel length, width, oxide thickness results in variation in threshold voltage of a device. The threshold voltage mismatch between the transistors on the SRAM array results in various failures such as read/write access and hold failures as well as have a strong impact on leakage of the SRAM array (Roy et al., 2003)[10]. The increase in leakage current through the transistor results in failure of the cell to retain the stored data causing the occurrence of hold failures. The reverse is true that is due to the presence of fault, leakage current increases which in turn increases power dissipation in the chip.

3.3 RC values at Nodes:

Each node say bit line or write line on applying signal have greater impact on the performance of the SRAM and have strong dependency on process parameters as well as operating conditions. For example by taking bit line capacitance into consideration several simulations are performed with capacitance varying from 0fF to 100fF with 10fF in steps and observed the power dissipation variation. Similarly overall node capacitance, resistance and delay values also observed in the parametric analysis for both faulty and fault free SRAM cell.

4. RESULTS AND COMPARISONS

The circuits for SRAM with read and write operations are developed using Micro wind Dsh2 simulation tool. The logic simulation options are selected such as Time unit in ns, the supply voltage 1.2v, with default gate delay 0.03ns, default wire delay 0.07ns. For the design of transistors default technology i.e. Current CMOS technology 0.12um is selected. In which length of transistor selected as 0.12um, and width is selected as 1.0um for NMOS and 2.0um for PMOS transistor.

Similarly for the layout diagrams, simulation was carried using Micro wind tool using Empirical Level 3 model at default room temperature 27 degrees centigrade with 6metal design rule. The results such as propagation delay, power dissipation and node values are obtained individually for read operation, write operation of SRAM and are tabulated in Table 1 and 2. The node values are compared individually between read and write values. Read and Write capacitance comparison is shown in fig.3. It is observed that read operation capacitance is less compare to write operation capacitance. Similarly resistance for read and operation also compared and is shown in fig.4.

Table 1 R, C values at various nodes in read circuit

Node	Cr,fF	Rr,Ω	Lenr, um	Lr,nH
!Q	4.46	6557	65	0.04
Q	1.43	3250	27	0.02
WL	2.07	369	30	0.02
BL	0.97	1158	20	0.01
!BL	1.07	2095	22	0.01

4.1 Simulation Results for SA0:

Case I: If gate and source of inverter NMOS transistor M3 are shorted leads to SA0, the corresponding layout is shown in fig 5, Node R,C values are shown in Table 3.
Case II: If drain and gate of access transistor M6 are shorted leads to SA0, the corresponding layout is shown in fig.6, Node R,C values are shown in Table 4.
Case III: If source and drain of access transistor M6 are shorted leads to SA0, the corresponding layout is shown in fig 7, Node R,C values are shown in Table 5.
Case IV: If drain and source of NMOS transistor M1 are shorted leads to SA0, the corresponding layout is shown in fig 8, Node R,C values are shown in Table 6.
Capacitance and Resistance variation with SA0 fault in different cases and their comparisons are shown in fig.9&10 respectively.

Table 2 R,C values at various nodes in write circuit

Node	Cw,fF	Rw,Ω	Lenw, um	Lw, nH
!Q	4.47	6728	67	0.04
Q	4.69	6248	68	0.04
WL	1.99	369	28	0.02
BL	0.93	1157	19	0.01
!BL	1.03	2095	22	0.01

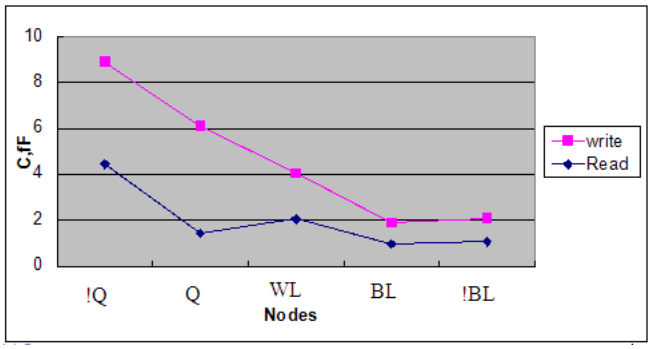

Fig -3 Comparison of read and writes capacitances at various nodes

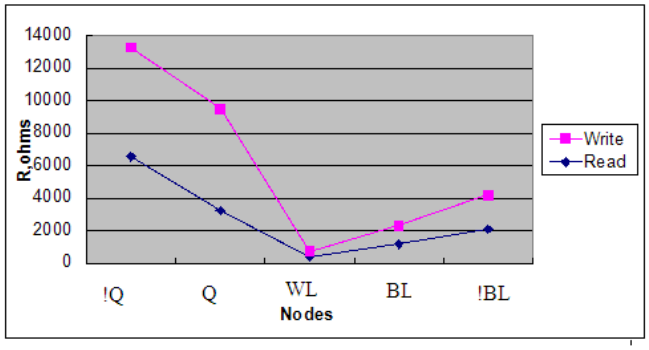

Fig -4 Comparison of read and writes resistances at various nodes

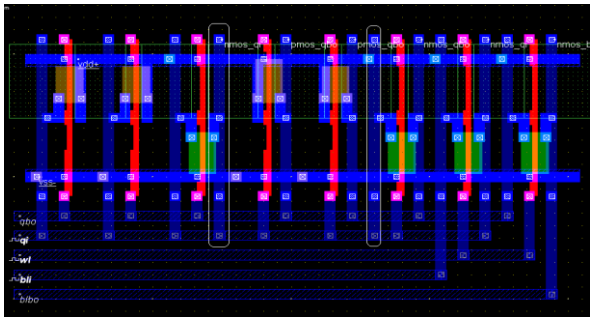

Fig -5 Layout for faulty cell with SA0 case I

Table 3 R,C values at various nodes with sa0 case I

Node	Cr01, fF	Rr01, Ω	Lenr01, um	Lr01,nH
!Q	4.49	6612	66	0.04
Q	5.73	9736	85	0.05
WL	1.99	369	28	0.02
BL	0.93	1157	19	0.01
!BL	1.03	2095	22	0.01

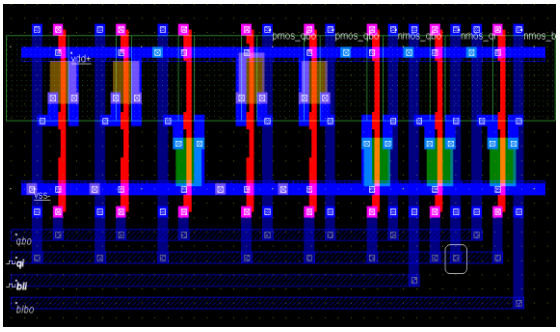

Fig -6 Layout for faulty cell with SA0 case II

Table 4 R, C values at various nodes with sa0 case ii

Node	Cr02,fF	Rr02, Ω	Lenr02, um	Lr02,nH
!Q	4.47	6728	67	0.04
Q	6 .26	6614	85	0.05
WL	6 .26	6614	85	0.05
BL	0.91	1157	18	0.01
!BL	1.01	2095	21	0.01

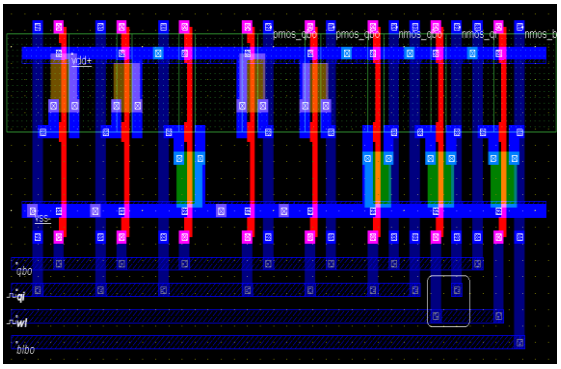

Fig -7 Layout for faulty cell with SA0 case III

Table 5 R, C values at various nodes with sa0 case iii

Node	Cr03, fF	Rr03,Ω	Lenr03, um	Lr03, nH
!Q	4.5	6612	66	0.04
Q	4.67	5552	67	0.04
WL	1.99	369	28	0.02
BL	1.01	2095	21	0.01
!BL	4.5	6612	66	0.04

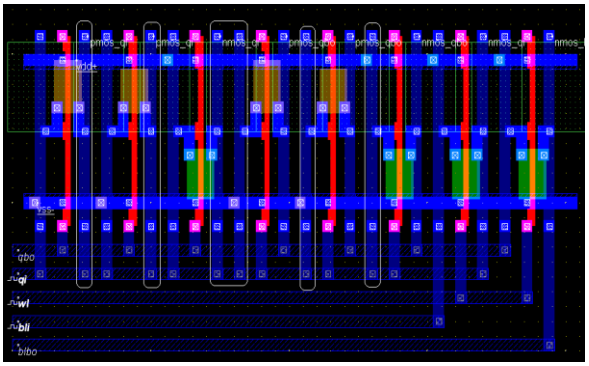

Fig -8 Layout for faulty cell with SA0 case IV

Table 6 R, C values at various nodes with sa0 case iv

Node	Cr04,fF	Rr04,Ω	Length, um	L, nH
!Q	4.46	6557	65	0.04
Q	7.75	15105	118	0.07
WL	1.99	369	28	0.02
BL	0.93	1157	19	0.01
!BL	1.03	2095	22	0.01

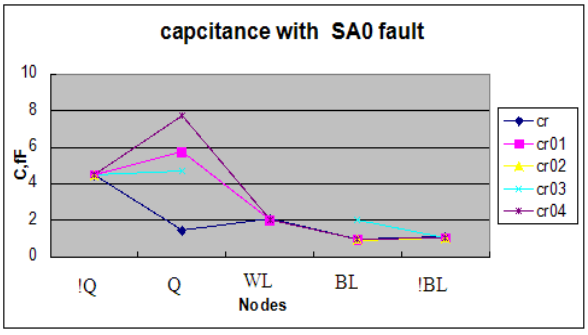

Fig -9 Comparison of Node capacitances between faulty (SA0) and fault free cell

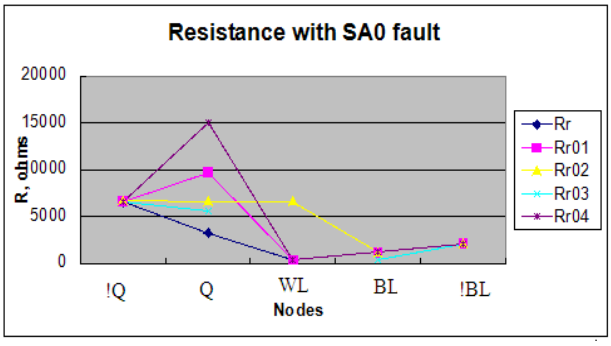

Fig -10 Comparison of Node Resistances between faulty (SA0) and fault free cell

4.2 Simulation Results for SA1:

Case I: If gate and source of inverter transistor M4 and gate and source of right access transistor M6 are together shorted leads to sa1 fault, the corresponding layout is shown in fig 11, Node R,C values are shown in Table 7.

Case II: If left Access transistor M5 gate and source are shorted leads to SA1 and the corresponding layout is shown in fig.12, Node R,C values are shown in Table 8.

Case III: If gate and drain of inverter transistor M2 and gate and source of access transistor M5 are shorted leads to SA1, the corresponding layout is shown in fig. 13, Node R,C values are shown in Table 9.

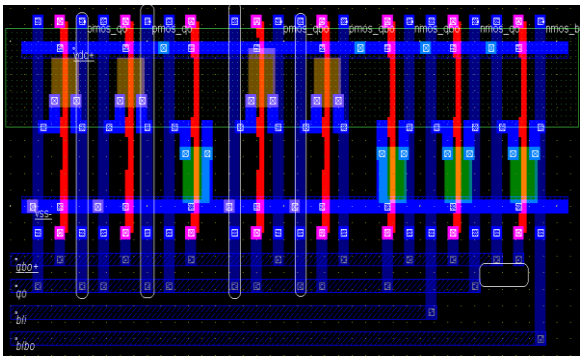

Fig -11 Layout for faulty cell with SA1 case I

Table 7 . R, C values at various nodes with sa1 case i

Node	Cr11, fF	Rr11,Ω	Lenr11, um	Lr11, nH
!Q	5.19	67195	74	0.04
Q	6.68	11391	101	0.04
WL	5.19	67195	74	0.04
BL	0.91	1157	18	0.01
!BL	1.01	2095	21	0.01

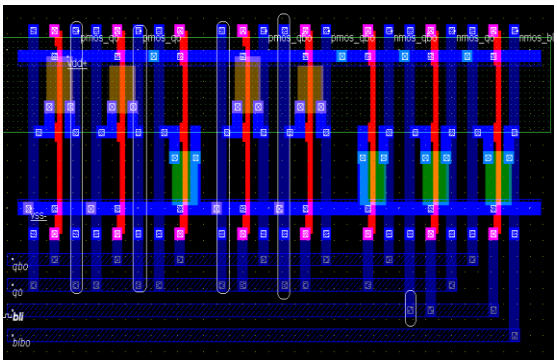

Fig -12 Layout for faulty cell with SA1 case II

Table 8 R, C values at various nodes with sa1 case ii

Node	Cr12,fF	Rr12,Ω	Lenr12, um	Lr12,nH
!Q	4.48	6557	65	0.04
Q	6.70	11858	101	0.06
WL	2.54	1524	37	0.02
BL	2.54	1524	37	0.02
!BL	1.01	2095	21	0.01

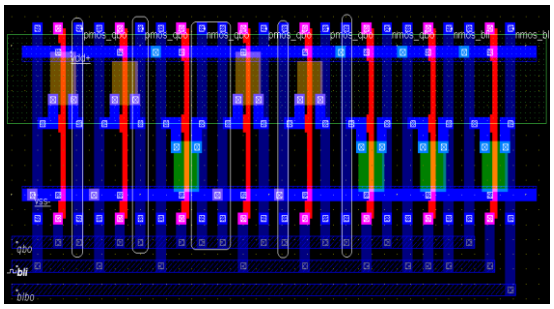

Fig -13 Layout for faulty cell with SA1 case III

Table 9 R, C VALUES AT VARIOUS NODES WITH SA1 CASE III

Node	Cr13,fF	Rr13, Ω	Len13, um	L13, nH
!Q	4.48	6557	65	0.04
Q	2.24	5370	39	0.02
WL	2.24	5370	39	0.02
BL	6.99	8012	98	0.06
!BL	1.01	2095	21	0.01

Capacitance and resistance variation with SA1 fault in different cases and their comparisons are shown in fig 14 & 15 respectively.

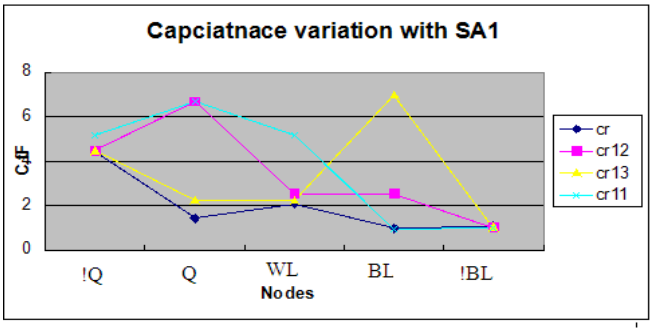

Fig -14 Comparison of Node capacitances between faulty (SA1) and fault free cell

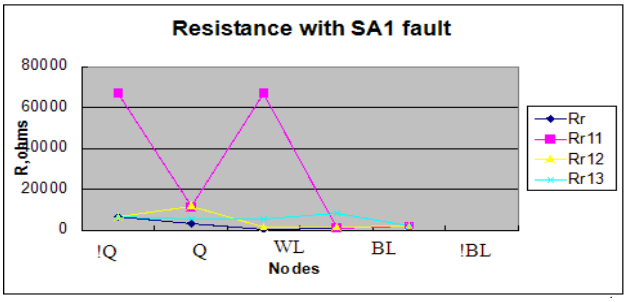

Fig -15 Comparison of Node Resistance between faulty (SA1) and fault free cell

5. CONCLUSION

Initially fault free SRAM cell was considered and found capacitance and resistance at each node. From the results it was observed that the capacitances for output of latch Q gives more capacitance i.e. 4.69fF when write operation was carried. Then !Q followed with next highest value i.e. 4.47fF. Whereas when read operation was performed, it was observed that capacitance at !Q is more i.e.4.46fF than Q and is 1.43fF. In both cases writing a '1' and reading a '1' is chosen.

We have proposed four cases for SA0 fault were considered and observed the corresponding R,C values at different nodes. The obtained node values for faulty cell were compared with fault free cell node R,C values. Similarly we proposed three cases for SA1 fault also. A defect-based fault analysis and defect simulation methodology has been presented. The simulation results show the existence of un-testable defects and un-modeled faults presented. The overall analysis with random R,C variations is much suitable for obtaining the better solutions towards improvement of the yield. The analysis is further can be extended by considering more complex faults such as transition and coupling faults.

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