AN OCTO CODING TECHNIQUE TO REDUCE ENERGY TRANSITION IN LOW POWER VLSI CIRCUITS

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Abstract

System on–chip design in deep submicron technology interconnects plays an important role in overall performance of the chip. Digital circuits consists of a number of interconnected logic gates which together perform a logic operation with more input signals. When an input signal changes the change will propagates via the gates to the circuit generating energy transition The signal transition causes to charge or discharge the capacitive load of CMOS circuits will induces the power dissipation. Recently power dissipation is becoming an important constrain in a deep submicron VLSI technology. There are several methods for the reduction of dynamic power dissipation through energy transition in data buses. Among them the Novel Octo-coding method is most effective and powerful method for enhancing the behavior of on-chip data buses. This coding method is implemented and analyzed using Xilinx and Modelsim tools

Keywords: *Switching activity, Hamming distance, Energy Transition, Active Power dissipation, Octo Coding .*

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1. INTRODUCTION

ENERGY Consumption is one of the major key aspects in the design of VLSI circuits [8] As the technology scales down to deep submicron technology, the bus energy reduction has become more and more important [9] so for all the researchers were worked on reducing transition activity on buses Bus invert coding [1], shift invert coding [3], Rotate coding [4], coding for energy reduction in VLSI interconnects [6].Low power design is becoming a new era in VLSI technology, as it impacts in many applications to optimize the power dissipation of digital systems in low power technology must be implemented through the design process from system level to process level. Power is a means of the rate of energy consumption. With the increase in speed , mobility and miniaturization of current electronic products power consumption has become major design factor, especially for hand held devices ,the power consumption determines the battery life time. therefore ,the designers and consumers of electronic devices as well as environmental considerations demand a reduction in power dissipation of digital circuits.

The rest of the paper is organized as follows: Definitions of some of the important terms are used in this paper are given in section II Bus Energy Model given in section III Power dissipation is given in section IV and a brief overview of the Related to bus coding is given in section V the proposed coding scheme is explained in section VI while Simulation and Results of proposed coding scheme with an example is shown in section VII , Finally conclusion are made in section VIII.

2. DEFINITIONS

Hamming Distance: The Hamming distance between the two code vectors is equal to the number of elements in which they differ.

Example:

Let X = 10111011
Let Y = 11110010

Hamming distance between X and Y is defined by;

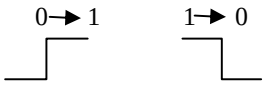
X = 1<u>0</u>11<u>1</u>011
Y = 1<u>1</u>110<u>0</u>10

Here only three bits are differ from each other ,

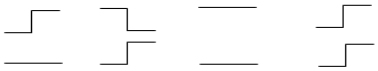
Hence Hd (X,Y) = 3

Energy Transition: It is defined as due to charging and discharging the data changed from 1 to 0 or from 0 to 1 vice versa between adjacent bus wires or on the same bus wire.

1. Transition between neighboring data on the same bus wire is called self Transition.



2. Transition between adjacent bus wire is called coupling Transition



3. BUS ENERGY MODEL

Figure1 shows a simplified bus model with parasitic capacitance and their voltages[2]. *Cs* is the self-capacitance from each bus line to ground, *Cc* is the coupling-capacitance between two adjacent bus lines and V_1, V_2 …are the node voltages.

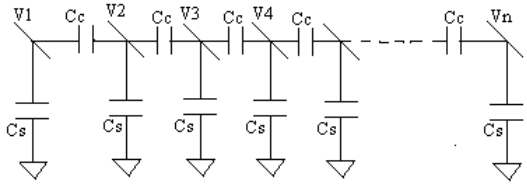


Fig-1 shows simple bus energy model

Let λ be the *capacitance factor* which is calculated as[2] the ratio between coupling capacitance to self capacitance. If the capacitance factor increases the technology will scale down.

$$\lambda = C_c / C_s \quad \text{----------(1)}$$

The energy saved due to the reduction of transitions is given in High performance data bus encoding technique in DSM technology[17] as

$$\text{Energy saved} = (1- T_{unc} / T_{cod}) *100 \text{ ----------(2)}$$

Where T_{unc} is the energy dissipated due to un encoded data transitions and T_{cod} is the energy dissipated due to coded data transitions.

Table-1 Shows Energy Transition analysis for self capacitance [15]

Transition of bits	State	Energy stored initially	Energy stored finally	Energy dissipated	Energy consumed
0→1	charge	0	$C_sV^2/2$	$C_sV^2/2$	C_sV^2
1→0	discharge	$C_sV^2/2$	0	$C_sV^2/2$	0

Table-2 Shows Energy Transition analysis for coupling capacitance [15]

Transition of bits	State	Energy stored initially	Energy stored finally	Energy dissipated	Energy consumed
00⟶ 00	-	0	0	0	0
00⟶ 01	charge	0	$C_cV^2/2$	$C_cV^2/2$	C_cV^2
00⟶ 10	charge	0	$C_cV^2/2$	$C_cV^2/2$	C_cV^2
00⟶ 11	-	0	0	0	0
01⟶ 00	discharge	$C_cV^2/2$	0	$C_cV^2/2$	0
01⟶ 01	-	0	0	0	0
01⟶ 10	Toggle	$C_cV^2/2$	$C_cV^2/2$	$2C_cV^2$	$2C_cV^2$
01⟶ 11	discharge	$C_cV^2/2$	0	$C_cV^2/2$	0
10⟶ 00	discharge	$C_cV^2/2$	0	$C_cV^2/2$	0
10⟶ 01	Toggle	$C_cV^2/2$	$C_cV^2/2$	$2C_cV^2$	$2C_cV^2$
10⟶ 10	-	0	0	0	0
10⟶ 11	discharge	$C_cV^2/2$	0	$C_cV^2/2$	0
11⟶ 00	-	0	0	0	0
11⟶ 01	Charge	0	$C_cV^2/2$	$C_cV^2/2$	C_cV^2
11⟶ 10	Charge	0	$C_cV^2/2$	$C_cV^2/2$	C_cV^2
11⟶ 11	-	0	0	0	0

4. POWER DISSIPATION

At the simplest level , there are two types of power that a designer cares about, static or leakage and active or dynamic switching power.

4.1 Active (Or) Dynamic Switching Power

It is the power consumed by the switching activity of the CMOS gates in a design .Power consumed by charging and discharging the interconnect capacitance

4.2 Static (or) Leakage Switching Power

It is the power consumed during the stand by mode of a design .CMOS gates typically have some amount of sub threshold leakage current even when gate are not turned on.

The drain to source leakage current is the main component of static power consumption .The leakage power was a very small part of the overall power consumption. In a typical chip 10% of the power consumed is leakage and 90% is dynamic power.

Instantaneous power $P(t) = i_{DD}(t)V_{DD}$ ----------(3)

Energy $E = \int_0^T p(t)dt = \int_0^T iDD(t)VDD\,dt$ ---(4)

Average power $P_{avg} = E/T$

$=1/T\int_0^T iDD(t)VDD\,dt$ -----(5)

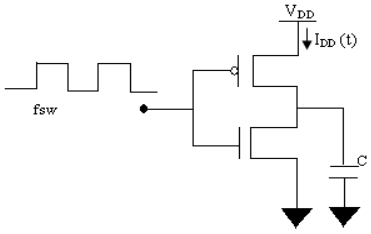


Fig-2 Shows CMOS inverter model for power calculation

Dynamic power is required to charge and discharge load capacitance when transistor switch. One cycle involves a rising and falling output.

1. On rising output , charge $Q = CV_{DD}$ is required .
2. On falling output , charge is dumped to ground

This repeats Tf_{sw} times over an interval of T

$$P_{dynamic} = 1/T\int_0^T iDD(t)VDD\ dt \text{ -------(6)}$$
$$= V_{DD}/T \int_0^T iDD(t)\ dt$$
$$= V_{DD}/T[\ T\ f_{sw}CV_{DD}\ ]$$

$$P_{dynamic} = CV_{DD}^2\ f_{sw} \text{ ----------(7)}$$

Suppose the system clock frequency is f,

Let $f_{sw} = \propto f$, where $\propto$ is the activity factor so,

$$P_{dynamic} = \propto C\ V_{DD}^2\ f \text{ ----------(8)}$$

5. RELATED WORK:

In recent years many research efforts in the switching activity have been introduce the power dissipation in VLSI circuits. There are two categories to reduce the power dissipation through switching activity. One category is used to reduce the switching activity in address buses. Among them A^2BC [16],The beach solution and gray coding . These methods used the redundancy bits to reduce the power dissipation

Another category is used to reduce the switching activity in data buses. Such techniques are bus invert coding [1] is the best method to reduce the self transitions. Bus regrouping [18] DSM bus invert coding [7] low power bus coding techniques considering inter wire capacitance[2], portioned bus coding for energy reduction [9] methods are efficient methods to reduce the coupling transitions coding for minimizing energy in VLSI interconnect [6] and an efficient switching activity reduction technique for on –chip data bus methods reduce both self and coupling transitions. but most of the methods consider only one type of encoding technique to reduce power dissipation .while this paper considers both self and coupling transitional activities to reduce the power dissipation by octo-encoding technique in an on – chip data buses.

6. PROPOSED CODING SCHEME

Let B^k be the n bit wide data present on the bus at time instant k is defined as $B^k = (b^k_{n-1}, b^k_{n-2}, \ldots b^k_1, b^k_2)$.. Let $B^{(k-1)enc}$ be the Reference data transmitted on the bus. Let d be the hamming distance between the buses. (Reference data and present data) M_d is the minimum hamming distance between the coded datas. Here input data has been chosen randomly and coded in eight different ways such as Invert, Swap, Invert even position, Invert odd position, Rotate left with invert, Rotate Right with invert, Circular Left Shift and Circular Right Shift. These methods had been separately discussed in various research papers, In this paper we combining all in a single suite named as octo Coding technique to code a 8 bit random data sample. Here the coding techniques are grouped as four, each having two coding methods. Hamming distance d is calculated for all the coding techniques. With respect to the minimum hamming distance, one coding technique is selected and another discarded in a group. Similarly the same technique is applied to the remaining three groups. Here from the eight coding techniques is reduced to four coding techniques. Again based on the already calculated minimum hamming distance, we chose one from the four coding techniques and the finally selected data will be transmitted to the decoder with three control bits for easy recovery. Figure 3 shows Octo coding Encoder block diagram ,it consists of three blocks such as octo coding , transition estimator and comparator.

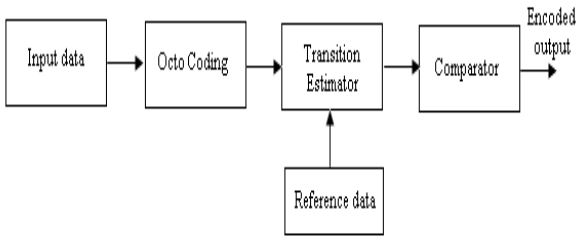


Fig-3 Shows Encoder of Octo coding Technique

6.1 Octo Coding

In this section the input data‘s are coded in eight different ways such as Invert, Swap, Invert even position, Invert odd position, Rotate left with invert, Rotate Right with invert, Circular Left Shift and Circular Right Shift. Then all are grouped in to four. Each group having two coding technique with 3 bit control signals are added to each coding technique to recover the original data at the decoder,

6.2 Transition Estimator

This block contains both hamming distance estimator and Transition counter to calculate the self and coupling transitions.

6.2.1 HD Estimator

This module separately calculates the hamming distance between the coded data and the reference data for each coding method then compare which coding method is having minimum hamming distance. By using this concept, among the eight, four methods are discarded and remaining four methods are again compared and the code having least hamming distance will be transmitted via bus.

6.2.2 Transition Counter

It consists of array of parallel adders used to compute number of self and coupling transitions occur during the data's transmitted via the data buses .Here we used only eight full adders to compute the transition count ,so we reduced 25 % of area compare to other existing encoding methods. The concept of parallel adders is used ,in order to minimize the critical delay.

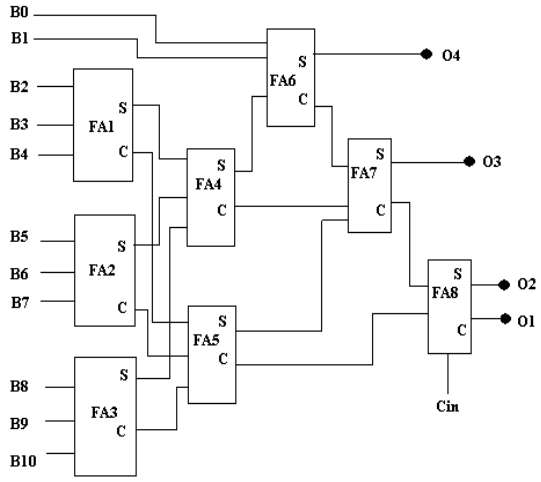


Fig-5 Shows Transition Estimator using Conventional CMOS Full adders

6.3 Comparator

Here four bit comparator used to compares the Hamming distance of the different methods and finds out the least among them. Since we are conditionally computing the hamming distance, for any case the comparator has to compare only three values. The inputs to this block are the encoded data along with its bit representation and its corresponding hamming distance. The output of this block is the encoded data with the least number of transitions and its 3-bit control signal. This encoded data is sent over the bus along with its 3-bit control signal.

Table-3 Shows Three Bit Control signal representation for Octo coding Technique

Sl.No	Coding Method	Control Bit
1	Invert	000
2	Swap	001
3	Invert Even Line	010
4	Invert Odd Line	011
5	Rotate Left with Invert	100
6	Rotate Right with Invert	101
7	Circular Left Shift	110
8	Circular Right Shift	111

Fig-4 Shows Decoder of Octo coding Technique

7. SIMULATION RESULT

The performance of proposed technique is designed by verilog language and the effectiveness of the coding is analyzed by using a modelsim simulator .Corresponding output is verified using 8 bit,16bit and 32 bit data buses with group of random sample vectors. Fig-6 shows simulation output for the 8 bit data bus with random sample.

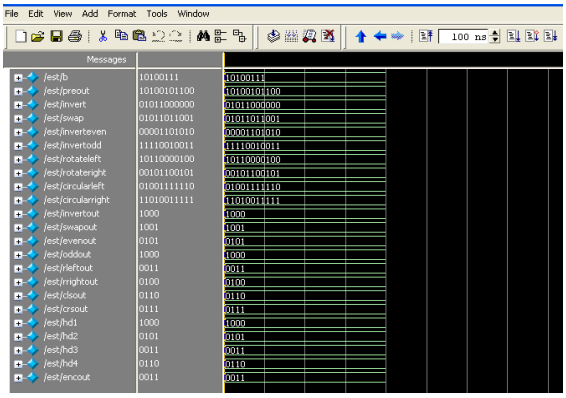


Fig-6 Shows simulation output of data 10100111

The Table-4. Illustrates performance analysis of energy transition among different encoding technique with respect to self and coupling transitions.

Table-4 Shows percentage of Transition Energy in different encoding methods

Sl.No	Coding method	Transition energy in %
1	Binv	41.41068
2	Dynamic	39.5557
3	Shinv	42.2474
4	Brg-HD	46.94077
5	Rotate	48.8903
6	Hdbc-DSM	45.55654
7	Novel	49.93060

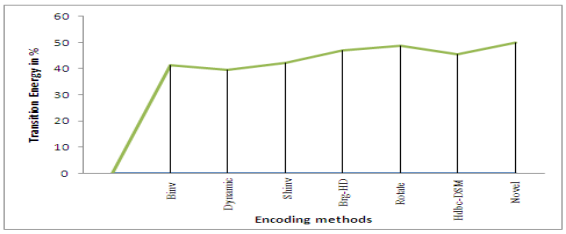


Chart-1 Shows percentage of Transition Energy in different encoding methods

CONCLUSIONS

We have successfully design and simulated Octo encoding technique to achieve energy reduction. The main goal of the proposed method is to reduce the overall transitions in DSM buses. The simulation results shows the overall reduced up to 49 % and also 1 % to 10% of energy reduction is achieved compare to other existing encoding methods. In this method the delay and glitches are not concentrated effectively. In future work these parameters will be considered very effectively to achieve a efficient energy reduction.

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