

LOW POWER AND HIGH PERFORMANCE DETFF USING COMMON FEEDBACK INVERTER LOGIC

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Abstract

The power consumption of a system is crucial parameter in modern VLSI circuits especially for low power applications. In this project, a low power Double Edge Triggered D-Flip Flop (DETFF) design is proposed in 65nm CMOS technology. The proposed DETFF is having less number of transistors than earlier designs. Simulations are carried out using HSPICE tool with different clock frequencies ranging from 400MHz to 2GHz and with different supply voltages ranging from 0.8V to 1.2V. In general, a power delay product (PDP)-based comparison is appropriate for low power portable systems. At nominal condition, the PDP of the proposed DETFF is improved by 65.48% and 44.85% over earlier designs DETFF1 and DETFF2 respectively. Simulation results show lowest power dissipation and least delay than existing designs, which claims that the proposed DETFF is suitable for low power and high speed applications.

Keywords: CMOS, flip-flops, Double-edge triggered, power dissipation, delay and PDP

1. INTRODUCTION

In recent years, consumer's attitudes are gearing towards better accessibility and mobility that caused a demand for an ever-increasing number of portable applications, requiring low-power dissipation and high throughput. For example, notebook, hand-held, palm-top computers are portable versions of microprocessors which require low power dissipation designs. In these applications, not only voice, but data as well as video are transmitted via wireless links. The weight and size of these portable devices is determined by the amount of power required. Low power design is very important to support these devices, particularly with respect to the integrated circuits, in which excessive power consumption will make the chip over heat and cause error or even permanent damage. The seriousness of this problem increases with the level of integration and thus we need to consider the power consumption of the chips for every component in the device. Hence, the major concerns of the VLSI circuit designer were low power dissipation, high speed, small silicon area, low cost and reliability. The battery lifetime for these products is crucial; hence, a well-planned low-energy consumption design strategy must be necessary.

The design for low power issues can't be overcome without precise power prediction and optimization tools. Therefore, there is a critical need for certain tools to calculate power dissipation during the design to meet the power constraints to ignore the costly redesign effort. Power dissipation is given by the equation, $P = \alpha CV^2f$. Voltage scaling is the most effective way to decrease power consumption, since power is

proportional to the square of the voltage. However, voltage scaling is associated with threshold voltage scaling which can cause the leakage power to increase exponentially. In order to reduce the complexity of circuit design, a large proportion of digital circuits are designed to be synchronous circuits. The power dissipation in synchronous VLSI circuits is contributed by several factors: i.e. I/O, logic and clock power dissipation. Clock power dissipation is divided into three major contributions: clock wires, clock buffers and flip-flops. Studies show that 40-45% of total power dissipated in integrated system is due to clock distribution network and 90% of which is consumed by the flip-flops and the last branches of the clock distribution network. D-type flip-flop's (DFF's) are one of the most fundamental building blocks in modern VLSI systems and it contributes a significant part of the total power dissipation of the system.

The most popular synchronous digital circuits are edge triggered flip-flops. Single-edge triggered (SET) flip-flops and Double-edge triggered (DET) are edge-sensitive devices, that is, data storage in these flip-flops occurs at specific edges of the clock signal. During each clock period, single-edge triggered flip-flops latch data at only one edge, either rising or falling edge of the clock signal. Double-edge triggered flip-flops latch data at both rising and falling edges of the clock signal during each period of the clock signal. Hence by using double-edge triggered flip-flops (DETFFs), the clock frequency can be significantly reduced - ideally, to half while preserving the rate of data processing. Using lower clock frequency may translate into considerable power savings for the clocked portions of a circuit.

The DETFF design aims at saving energy both on the clock distribution network (by halving the clock frequency) and flip-flops. It is preferable to reduce circuits' clock loads by minimizing the number of clocked transistors. A simple DETFF is implemented with about 50% extra transistors than the traditional SET flip flop, however, this issue is being resolved in recent intensive researches. It motivates to use DETFF for larger and complicated designs, especially for application specific integrated circuits (ASIC) design. Several DET flop-flops have been proposed in the literature. The main attention has been in improving the performance of the circuits.

This paper is organized as follows: Section II explains the DETFF structures consist of conventional and proposed DETFF circuits. The nominal simulation conditions along with transient analysis and optimization performed during simulation are discussed in Section III. Section IV consists of Results and performance of proposed design and conventional designs comparisons in terms of average power dissipation, delay and PDP. Paper ends with the conclusion.

2. DOUBLE EDGE TRIGGERED FLIP FLOP STRUCTURES

There are several ways to implement a DETFF; In general they can be categorized into two ways. The first idea is to insert additional circuitry to generate internal pulse signals on each clock edge. The second idea is to duplicate the pathway to enable the flip-flop to sample data on every clock edge. The same data throughput can be achieved with half of the clock frequency by using DETFF. In other words double edge clocking can be used to save half of the power on the clock distribution network.

2.1 Conventional Double-Edge Triggered Flip-Flops

The DET flip flop given in [1] is shown in figure 1. This flip-flop is basically a Master Slave flip-flop structure and has two data paths. The upper data path consists of a Single Edge Triggered flip-flop (SETFF) implemented using transmission gates. It employs positive edge. The lower data path consists of a negative edge triggered flip-flop implemented using transmission gates. Both the data paths have feedback loops connected such that whenever the clock is stopped, the logic level at the output is retained. This flip-flop has 22 transistors excluding clock driver. In these 22 transistors, 12 transistors are clocked transistors.

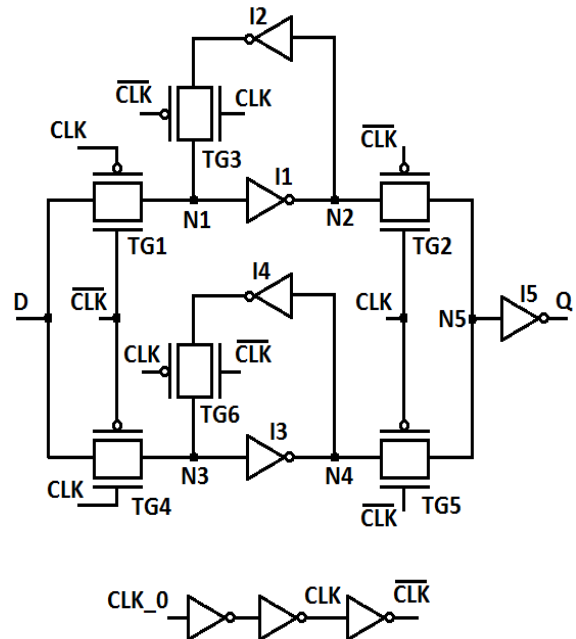


Fig -1: DETFF1 given in [1]

The figure 1 shows a pair of parallel loops. When the clock pulse changes from low to high, the upper loop holds data and the down loop samples data. But when the clock pulse changes from high to low, the top loop switches to sample data and then the down loop switches to hold data.

The DET flip flop given in [2] is shown in figure 2. This flip-flop is also basically a Master Slave flip-flop structure and consists of two data paths. The transmission gates (TG) in both the data path are clocked such that the upper data path works as positive edge triggered flip flop and lower data path works as negative edge triggered flip flop. The upper data path consists of transmission gates TG1, TG2 and inverter I1. The lower data path consists of transmission gates TG3, TG4 and inverter I3.

The input data is connected to TG1 and TG3 and the output is taken from inverter I5 whose input is connected with TG2 and TG4. Both the data paths have feedback loops connected such that whenever the clock is stopped, the logic level at the output is retained so as to maintain the static functionality. The feedback in upper data path consists of an inverter I2 and a pass transistor P1. The feedback in lower data path consists of an inverter I4 and a pass transistor P2. This design is identical to figure 1 except feedback path. The feedback transmission gates of figure 1 are not on critical paths and replaced with pass transistors. This flip-flop has 20 transistors excluding clock driver. In these 20 transistors, 10 transistors are clocked transistors.

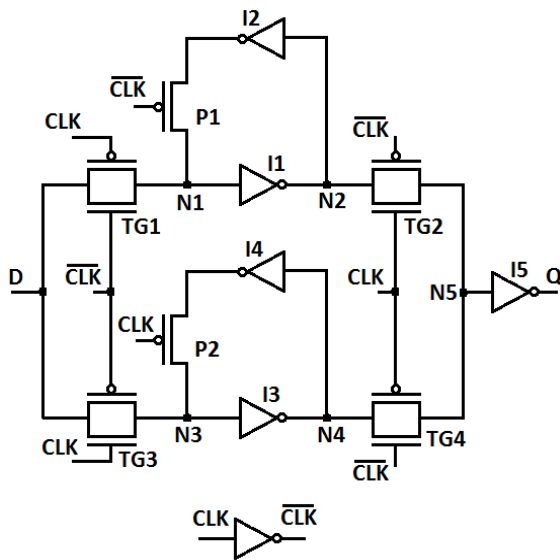


Fig -2: DETFF2 given in [2]

2.2 Proposed Double-Edge Triggered Flip-Flop

The proposed DET Flip-Flop design is shown in figure 3. This flip-flop is also basically Master Slave flip-flop structure and it consists of two data paths. The upper data path consists of transmission gate TG1, pass transistors (P1, P2) and an inverter I1. The lower data path consists of transmission gate TG2, pass transistors (P3, P4) and an inverter I2. The transmission gate and pass transistors in both the data paths are clocked such that the upper data path works as positive edge triggered flip flop and lower data path works as negative edge triggered flip flop. The inverter I3 serves as a common feedback inverter and the output of the inverter I4 forms the output of the present invention.

This design is identical to figure 1 except feedback path has been changed and the number of clocked transistors is reduced by using n-type pass transistors instead of transmission gates. The transmission gates TG2, TG3, TG5, and TG6 of figure 1 are replaced with pass transistors P1, P2, P3 and P4 respectively. Basically n-type pass transistors give weak high but in figure 3, the n-type pass transistors are followed by an inverter, which results in strong high. Thus the proposed DETFF in figure 3 is free from threshold voltage loss problem of pass transistors. The feedback network of figure 2 is altered by placing the n-type pass transistor instead of p-type pass transistor. Since, the area incurred by NMOS is less than that of PMOS transistor in order to compensate the mobility constraint of NMOS and PMOS transistors.

According to the DETFF1 and/or DETFF2, one of two loops always samples the data and the other loop always holds the data. Therefore, only a single feedback loop is required to hold the data. The proposed DETFF design eliminates one feedback loop and reduces the number of transistors compared to the

existing designs. The two inverters I2 and I4 of figure 1 are used for two feedback paths, but here a single feedback inverter I3 is used as a common feedback inverter for two feedback paths as shown in figure 3.

The input data is supplied to one end each of two transmission gates (TG1, TG2). The other ends of the two transmission gates (TG1, TG2) are separately connected to the input of two inverters (I1, I2). The outputs of the two inverters (I1, I2) are separately connected to the inputs of another two inverters (I3, I4) via the pass transistors (P1, P3). The output of inverter I3 goes through two pass transistors (P2, P4) to connect to one end of the above mentioned two transmission gates (TG1, TG2) separately, and the output of the inverter I4 forms the output of the present invention. Both the data paths have feedback loops connected such that whenever the clock is stopped, the logic level at the output is retained so as to maintain the static functionality.

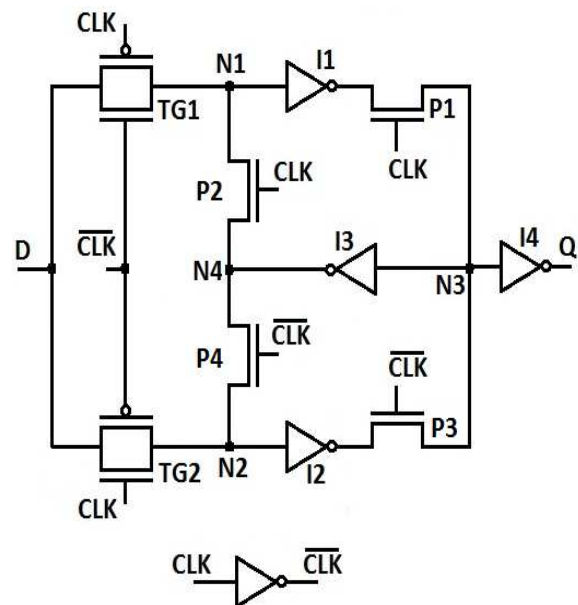


Fig -3: Proposed DETFF

The novelty of the proposed flip flop lies in the feedback strategy using common feedback inverter and pass transistors to make the design static. This improves the power efficiency of the proposed flip flop. This flip flop has 16 transistors excluding clock driver. In these 16 transistors, 8 transistors are clocked transistors. It is preferred to reduce number of clocked transistors to achieve low power dissipation. So, the main advantages of the proposed design are low power dissipation and increased performance with low transistor count. Thus the proposed Double Edge Triggered Flip-Flop (DETFF) has become more efficient in terms of area, power and speed which claim for better performance than conventional designs.

3. SIMULATIONS AND TRANSIENT ANALYSIS

Simulation parameters used for comparison are shown in Table 1. For a fair comparison we simulated all flip-flops on same simulation parameters.

Table -1: CMOS Simulation parameters

Technology	65nm CMOS
MOSFET Model	BSIM 4
Nominal Conditions	Vdd =1V, T=25° C
Duty Cycle	50 %
Nominal Clock Frequency	400MHz
Data Rate at Nominal Clock Frequency	800Mbps

All simulations are carried out using HSPICE simulation tool at nominal condition with different range of frequencies from 400MHz to 2GHz and with different range of supply voltages from 0.8V to 1.2V. The simulated waveform for the proposed DET flip-flop at nominal condition is shown in figure 4. This waveform shows that the DETFF is storing the data in both rising edge and falling edge of the clock signal.

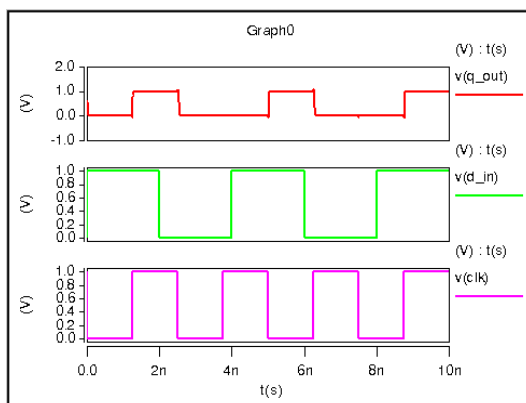


Fig -4: Output waveform for proposed DETFF

We have optimized the transistor sizes. The transistors, that are not located on critical path, are implemented with minimum size. We have improved the feedback path in our design. We simulated the design to achieve minimum power-delay (clk-q) product (PDP). Transistor count is also included to maintain a fair level of comparisons. In DETFF1 there are 12 clocked transistors, in DETFF2 there are 10 clocked transistors while in our design there are only 8 clocked transistors. We have reduced the number of clocked transistors. Thus we have reduced the power dissipation. The switching power, which is dominant power, is proportional to the square of the supply voltage. We have reduced supply voltage to 1V or even less voltages for the reduction of the power.

4. PERFORMANCE COMPARISON

The performance of the proposed DETFF is evaluated by comparing the average power dissipation, delay and PDP with DETFF 1 and DETFF 2. Comparison of simulation results at nominal condition for the three FFs is summarized in Table 2.

Table -2: Comparison of simulation results for the three FFs at nominal condition

Specification	DETFF 1	DETFF 2	Proposed DETFF
Average Power Dissipation (μ W)	1.471	1.066	0.881
Clk-Q Delay (ps)	26.47	22.86	15.26
PDP (10-18J)	38.94	24.37	13.44
PDP Improvement % over 1	----	37.42	65.48
No. of Transistors (excluding clock driver)	22	20	16

Since D to Q delay depends on when the data transition occurs, here we measured clock to Q delay. The clock-to-Q delay is the delay from the active clock input to the new value of the output. We simulated all DETFFs with different clock frequencies ranging from 400MHz to 2GHz and with different supply voltages ranging from 0.8V to 1.2V. Each flip-flop is optimized for power delay product. In general, a PDP-based comparison is appropriate for low power portable systems in which the battery life is the primary index of energy efficiency.

Table 3 shows the PDP of all three flip flops at different supply voltages, this indicates that the proposed design has an average improvement of 65.28% and 45.98% in terms of PDP as compared to DETFF1 and DETFF2 respectively. Table 4 shows the PDP of all three flip flops at different clock frequencies, this indicates that the proposed design has an average improvement of 70.82% and 44.25% in terms of PDP as compared to DETFF1 and DETFF2 respectively. Chart 1 and chart 2 show the statistical variation of PDP for all the 3 flip-flops on varying supply voltage and clock frequency respectively. This shows our design is suitable for low power dissipation and high performance applications.

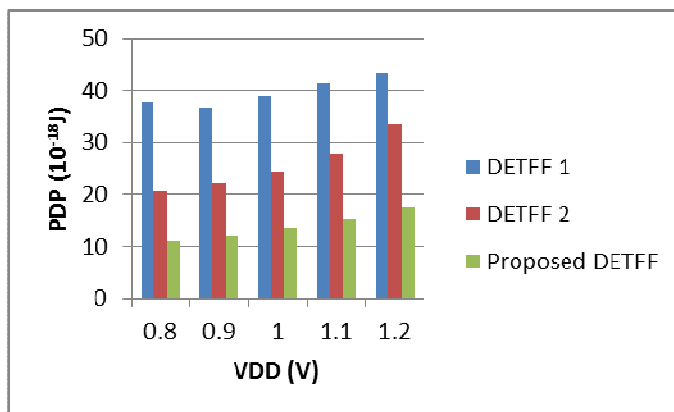
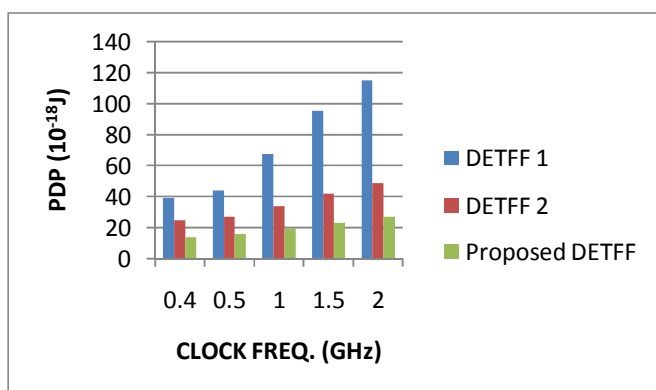
Table -3: PDP of 3 FFs with the variation of supply voltage

VD D (V)	DETF F 1 (10-18J)	DETFF 2 (10-18J)	Proposed DETFF (10-18J)	Improv ement % Over 1	Improve ment % Over 2
0.8	37.84	20.81	11.06	70.77	46.85

0.9	36.8	22.09	12.04	67.28	45.5
1.0	38.94	24.37	13.44	65.48	44.85
1.1	41.3	27.85	15.25	63.07	45.24
1.2	43.54	33.32	17.51	59.78	47.45

Table-4: PDP of 3 FFs with the variation of clock frequency

Clock Freq. (GHz)	DETF F1 (10-18J)	DETF F 2 (10-18J)	Proposed DETFF (10-18J)	Improve ment % Over 1	Improve ment % Over 2
0.4	38.94	24.37	13.44	65.48	44.85
0.5	43.84	26.92	15.52	64.6	43.46
1.0	67.47	33.89	19.2	71.54	43.35
1.5	95.09	41.54	22.94	75.87	44.78
2.0	114.69	48.55	26.8	76.63	44.8

**Chart -1:** Statistical variation of PDP for the 3 FFs on varying supply voltage**Chart -2:** Statistical variation of PDP for the 3 FFs on varying clock frequency

CONCLUSIONS

The proposed Double-edge-triggered D flip-flop is a low power, low voltage, high speed and low transistor count flip-flop designed in 65nm CMOS technology. This is static in nature. The proposed DETFF design eliminates one feedback loop by using common feedback inverter logic thereby reducing the number of transistors and also by using pass transistors the number of clocked transistors is reduced compared to the existing DET flip flops. This improves the power efficiency of the proposed DETFF. The three DET flip-flops are simulated with different supply voltages ranging from 0.8V to 1.2V and with different clock frequencies ranging from 400MHz to 2GHz. At nominal condition, the PDP of the proposed DETFF is improved by 65.48% and 44.85% over earlier designs DETFF1 and DETFF2 respectively. Simulation results show that the proposed design has lowest power dissipation and least delay thereby it has lowest PDP than existing designs. Therefore the proposed design is very well suited for low power and high speed applications operating at low voltages.

REFERENCES

- [1] M. Pedram, Q. Wu, and X. Wu, "A New Design of Double Edge Triggered Flip-Flops," Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 417–421, 1998.
- [2] Imran Ahmed Khan, Danish Shaikh and Mirza Tariq Beg, "2 GHz Low Power Double Edge Triggered flip-flop in 65nm CMOS Technology" IEEE Conference, pp 978-1-4673-1318-6/12, 2012.
- [3] Xiaowen Wang, and William H. Robinson, "A Low-Power Double Edge-Triggered Flip-Flop with Transmission Gates and Clock Gating" IEEE Conference , pp 205-208, 2010.
- [4] Hossein Karimiyan Alidash, Sayed Masoud Sayedi and Hossein Saidi, "Low-Power State-Retention Dual Edge-Triggered Pulsed Latch," Proceedings of ICEE 2010, May 11-13, IEEE 2010.
- [5] Peiyi Zhao, Jason McNeely, Pradeep Golconda and Jianping Hu, "Low Power Design of Double-Edge Triggered Flip-Flop by Reducing the Number of Clocked Transistors," IEEE Conference, 2008.
- [6] Yu Chien-Cheng, "Design of Low-Power Double Edge-Triggered Flip- Flop Circuit", Second IEEE Conference on Industrial Electronics and Applications, pp 2054-2057, 2007.
- [7] Ahmed Sayed and Hussain Al-Asaad, "A New Low Power High Performance Flip-Flop" IEEE Conference, pp 723-726, 2006.
- [8] Nikola Nedovic, Mark Aleksic and Vojin G. Oklobdzija, "Comparative Analysis of Double-Edge Versus Single-Edge Triggered Clocked Storage Elements" IEEE Conference, pp V-105 to V-108, 2002.

- [9] Chandrakasan, W.Bowhill, and F. Fox, "Design of High-Performance Microprocessor Circuits", 1st ed. Piscataway, NJ: IEEE, 2001.
- [10] G. E. Tellez, A. Farrahi, and M. Sarafzadeh, "Activity-Driven Clock Design for Low Power Circuits," Proceedings of the IEEWACM International Conference on Computer-Aided Design (ICCAD), pp. 62- 65, 1995.

BIOGRAPHIES



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