

STUDY OF SINUSOIDAL AND SPACE VECTOR PULSE WIDTH MODULATION TECHNIQUES FOR A CASCADED THREE-LEVEL INVERTER

Chunduri Sreeharsha¹, Anurag Das², Srinivasan Pradabane³

^{1,2} Student, ³ Assistant Professor, Dept. of Electrical Engineering, NITW, AP, India
 sreeharsha.chunduri@gmail.com, anuragdas16@gmail.com, spradabane@nitw.ac.in

Abstract

This paper compares and evaluates the performance of Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SVPWM) techniques for a three-level inverter by cascading two two-level inverters. In this topology, four power semiconductor switches are used per phase and a total of twelve switches are required. The simulation study shows that SVPWM is superior to SPWM in the aspects of better DC-bus utilization and offering better spectral performance.

Index Terms: space vector modulation, multi-level inverters, sine-triangle modulation, and cascaded inverter

1. INTRODUCTION

In recent decades there has been a large number of variable speed induction motor drives which serves many industrial applications such as fans, pumps, machine tool cutting, steel rolling mills, etc.,. Voltage source inverters are employed for these drives as there is a dramatic increase in the power semiconductor technology which offers power ratings from few hundred watts to several megawatts. Voltage source inverters produce pulsed output waveforms, consisting of the fundamental component which is required to drive the motor, as well as harmonics which contribute only to the losses and torque pulsations. Ever since the invention of multilevel inverter topology namely Neutral-point clamped multilevel inverter in 1981 [1], various three-level inverter topologies such as the capacitor-clamped inverters, H-bridge inverters and cascaded inverters have been proposed [2-4]. Cascaded multilevel inverter topology has been proposed by Somasekhar et. al. [5] by connecting two two-level inverters in cascaded scheme

In this paper, a comparison is made with the two multi-carrier PWM techniques namely sinusoidal pulse width modulation and space vector pulse width modulation schemes pertaining to cascaded three-level inverter and the comparative analysis using MATLAB/Simulink is presented and the results signify that SVPWM is better than SPWM.

2. THREE-LEVEL CASCADED MULTILEVEL INVERTER

Fig-1 shows the cascaded three-level inverter topology. The circuit configuration for a three-level cascaded inverter is

obtained by connecting the output of the first inverter to DC input points of the corresponding phases in inverter-2 as shown in Fig-1. Here, both the top and bottom inverters are operated with isolated DC power supplies.

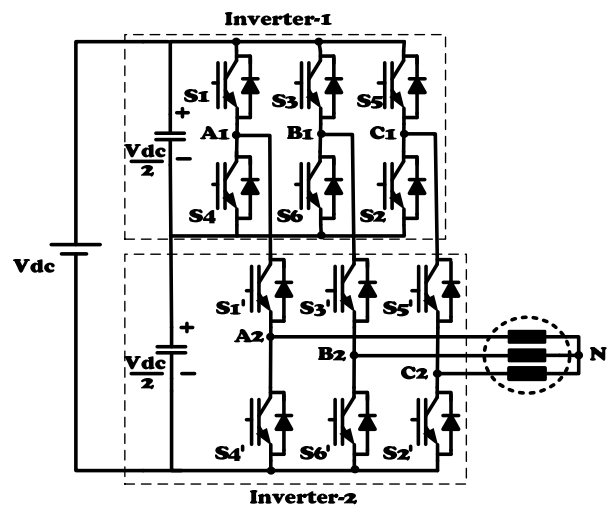


Fig-1: Cascaded Three-level Inverter Scheme

The pole voltage of inverter-1 with respect to point 'O' are denoted by V_{A1O} , V_{B1O} , V_{C1O} respectively and the pole voltages of the second inverter is denoted by V_{A2O} , V_{B2O} and V_{C2O} respectively. The pole voltage of any phase of inverter-2 attains a voltage of $V_{dc}/2$ if the top switch of that leg in inverter-2 is switched-ON and the bottom switch of the corresponding leg of the inverter-1 is switched-ON. Similarly, the pole voltage of any phase of inverter-2 attains a voltage of

V_{dc} if the top switch of that leg in inverter-2 and the top switch of the corresponding leg in inverter-1 is switched-ON. Thus the DC input points of the individual phases of inverter-2 may be connected to a DC link voltage of either V_{dc} or $V_{dc}/2$ by switching ON the top switch or the bottom switch of the corresponding phase leg in inverter-1. The pole voltage of a given phase of inverter-2 attains a voltage of zero, if the bottom switch of the corresponding leg in inverter-2 is switched ON. In this case, the DC input point of that phase of inverter-2 is floating as the top and bottom switches are switched complementarily in any leg in a two-level inverter. Thus the pole voltage of a given phase for inverter-2 is capable of assuming one of the three possible values $0, V_{dc}/2$ and V_{dc} which is the characteristic of a three-level inverter.

3. PWM SCHEMES FOR CASCADED THREE-LEVEL INVERTER

Pulse Width Modulation (PWM) technique conforms the width of the pulse, formally the pulse duration based on the modulating signal. In inverter circuits, the PWM is a bit complex as the desired inverter output is to be sinusoidal with magnitude and frequency control. Sine-triangle Pulse Width Modulation (SPWM) is one of the many popular PWM schemes. In any type of PWM scheme there is a modulating or reference wave and a carrier wave. There are different types of modulation strategies. This article will present the theory and implementation of SPWM and Space Vector Pulse Width Modulation (SVPWM).

3.1 Sine-Triangle PWM Technique

The principle of the sinusoidal PWM scheme for the two-level inverter is illustrated in Fig-2, where $V_{mA}, V_{mB},$ and V_{mC} are the three-phase sinusoidal modulating waves and V_{cr} is the triangular carrier wave. The fundamental frequency component in the inverter output voltage can be controlled by amplitude modulation index,

$$m_a = V_m / V_{cr} \tag{1}$$

where V_m and V_{cr} are the peak values of the modulating and carrier waves, respectively. The amplitude modulation index m_a is usually adjusted by varying V_m while keeping V_{cr} fixed. The frequency modulation index is defined by

$$m_f = f_m / f_{cr} \tag{2}$$

where, f_m and f_{cr} are the frequencies of the modulating and carrier waves, respectively.

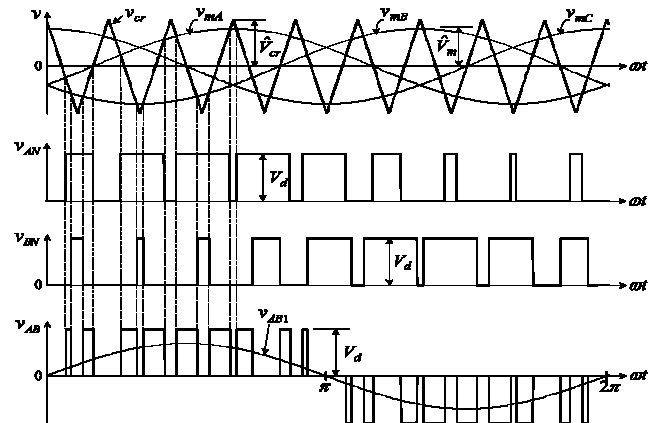


Fig-2: Sine-triangle PWM Scheme

The gating signals for a conventional two-level inverter using SPWM can be derived as follows. The operation of switches S1 to S6 is determined by comparing the modulating waves with the carrier wave. When $V_{mA} \geq V_{cr}$, the upper switch S1 in inverter leg A is turned on. The lower switch S4 operates in a complementary manner and thus is switched off. The resultant inverter terminal voltage V_{AN} , which is the voltage at the phase A terminal with respect to the negative DC-link bus ‘N’, is equal to the DC voltage V_d . When $V_{mA} < V_{cr}$, S4 is on and S1 is off, leading to $V_{AN} = 0$. Since the waveform of V_{AN} has only two levels, V_d and 0, the inverter is known as a two-level inverter.

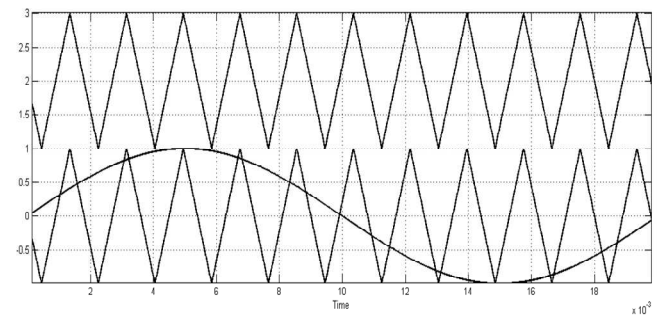


Fig-3: Sine-Triangle PWM Scheme for Cascaded Three-Level Inverter Scheme

It should be noted that to avoid possible short circuit during switching transients of the upper and lower devices in an inverter leg, a blanking time should be implemented, during which both switches are turned off. For an m-level inverter, m-1 carriers with the same frequency and same peak-to-peak amplitude are disposed such that the bands they occupy are contiguous. Fig-3 shows the variation of the modulating waveform with respect to the two-level and three-level inversion.

3.2 Space-Vector PWM Technique

Space Vector Modulation (SVM) is one of the popular real-time Pulse Width Modulation (PWM) techniques and is widely used for digital control of Voltage Source Inverters (VSI). The operating status of all the switches in a two level inverter can be represented as Switching State '+' which denotes that the upper switch in inverter leg is ON and the inverter voltage (V_{AN}, V_{BN}, V_{CN}) is $+V_{dc}$ while '-' indicates that the inverter terminal voltage is zero due to the conduction of lower switch. There are eight possible combinations of switching states in two level inverters. For example, the switching state '1' (+--) corresponds to the conduction of switches S1, S6 and S2 in the legs A, B and C respectively. Among the eight switching states '7' (+++) and '8' (---) are zero states and others are active states.

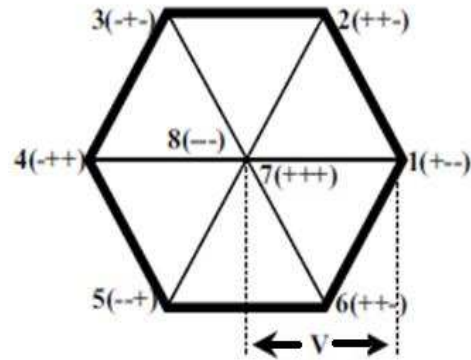


Fig-4: Space vector diagram of a two level inverter

Table -1: Space Vector Switching States

Space Vector	Switching States	ON-state Switch	Vector Definition	
Zero Vectors, V_0	7(+++)	S_1, S_3, S_5	$V_0 = 0$	
	8(---)	S_2, S_4, S_6		
Active Vectors	V_1	1 (+--)	S_1, S_6, S_2	$V_1 = (2/3)V_d e^{j0}$
	V_2	2 (++-)	S_1, S_3, S_2	$V_2 = (2/3)V_d e^{j\pi/3}$
	V_3	3 (-+-)	S_4, S_3, S_2	$V_3 = (2/3)V_d e^{j2\pi/3}$
	V_4	4 (-++)	S_4, S_3, S_5	$V_4 = (2/3)V_d e^{j3\pi/3}$
	V_5	5 (--+)	S_4, S_6, S_5	$V_5 = (2/3)V_d e^{j4\pi/3}$
	V_6	6 (+++)	S_1, S_6, S_5	$V_6 = (2/3)V_d e^{j5\pi/3}$

The active states and zero states are denoted by their respective space vectors, where the six active vectors V_1 to V_6 form a regular hexagon with six equal sectors (1-6) as shown in Fig-4 with its centre 'O' with the location of two zero vectors.

To obtain the relationship between the space vector and the switching states, the inverter is assumed to be in three phase balanced operation. Then we have,

$$V_{AO}(t) + V_{BO}(t) + V_{CO}(t) = 0 \tag{3}$$

Where V_{AO}, V_{BO} and V_{CO} are the instantaneous load phase voltage In a balanced three phase system, if the two quantities are known, then the other quantity can be easily determined.

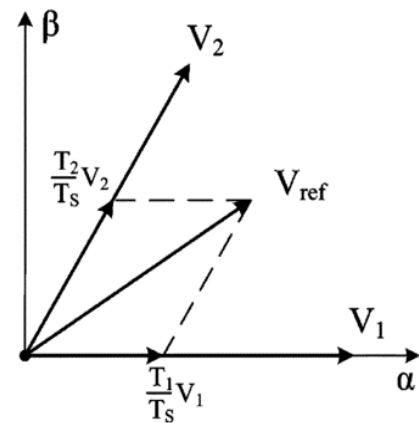


Fig-5: Space vector realization and switching time calculations

A space vector can normally be expressed in terms of two phase voltage in the α - β plane as shown in Fig 3.

$$V(t) = V_{\alpha}(t) + jV_{\beta}(t) \tag{4}$$

Substituting (2) in (1),

$$V(t) = 2/3[V_{AO}(t) e^{j0} + V_{BO}(t) e^{j2\pi/3} + V_{CO}(t) e^{j4\pi/3}] \tag{5}$$

where $e^{jx} = \cos(x) + jsin(x)$ and $x = 0, 2/3$ or $4/3$.

For active state 1(+--):

$$V_{AO} = 2V_{DC}/3; V_{BO} = -V_{DC}/3; V_{CO} = -V_{DC}/3 \tag{6}$$

The corresponding space vector can be obtained by substituting (4) into (3),

$$V_1 = 2V_d e^{j0} \tag{7}$$

In the similar way,

$$V_k = 2 V_{DC} e^{j(k-1)\pi/3} \tag{8}$$

where $k = 1, 2, \dots, 6$ respectively.

The two zero states 7(+ + +) and 8(- - -), are located at the same vector location as shown in the figure. By exploiting the redundancy of the null vectors, a centre-spaced switching can be obtained which reduces the switching in a particular sample. It is to be noted that the active and zero states do not move in space and thus they are referred to as stationary vectors. On the contrary, V_{ref} as in fig 3, rotates in space with angular velocity $\omega=2\pi f$, and f being the frequency the output voltage.

For a given magnitude (length) and position, V_{ref} can be synthesized by three nearby stationary vectors based on which the switching states of the inverter can be selected and gate signals for the active switches are generated. As V_{ref} traverses through different sectors one by one, different sets of switches will be turned ON and OFF. As a result, when V_{ref} rotates one revolution in space, the inverter output voltage varies one cycle over time. The inverter output frequency corresponds to the rotating speed of V_{ref} , while its output voltage can be adjusted by the magnitude of V_{ref} .

3.2 Dwell Time Calculation

From figure 4 and 5, consider sector-1. Let T_1, T_2 and T_0 be the dwelling times for the vectors V_1 (+-), V_2 (++), V_0 (+++, ---) respectively. Then according to volt-sec balance

$$V_S T_S = V_1 T_1 + V_2 T_2 + V_0 T_0 \tag{9}$$

Sampling time (T_S),

$$T_S = T_1 + T_2 + T_0 \tag{10}$$

But the vectors V_1, V_2 and V_3 can be expressed as $V_0 = 0; V_1 = (2/3) V_{DC}; V_2 = (2/3) V_{DC} e^{j\pi/3}$

Splitting equation-1 into components in α - β plane, we get

$$V_S T_S \cos \alpha = V_1 T_1 + V_2 \cos(60) T_2 \tag{11}$$

$$V_S T_S \sin \alpha = V_2 \sin(60) T_2 \tag{12}$$

$$|V_1| = |V_2| = (2/3) V_{DC} \tag{13}$$

Substituting this value in equations 2 and 3 and solving them we get

$$T_1 = \sqrt{3} (V_S T_S / V_{DC}) \sin(\pi/3 - \alpha) \tag{14}$$

$$T_2 = \sqrt{3} (V_S T_S / V_{DC}) \sin(\alpha) \tag{15}$$

$$T_0 = T_S - T_1 - T_2 \tag{16}$$

Where $0 \leq \alpha \leq \pi/3$. This is valid if the reference vector is in the first sector. For any k^{th} sector the α in general is given by

$$\alpha - (k-1) \pi/3 \tag{17}$$

The modulation index, $m_a = \sqrt{3} V_S / V_{DC}$ (18)

In order to reduce the switching loss an optimum switching must be undertaken. It is accomplished by sandwiching the effective time period in between the null states' times period which is shown in figure 7.

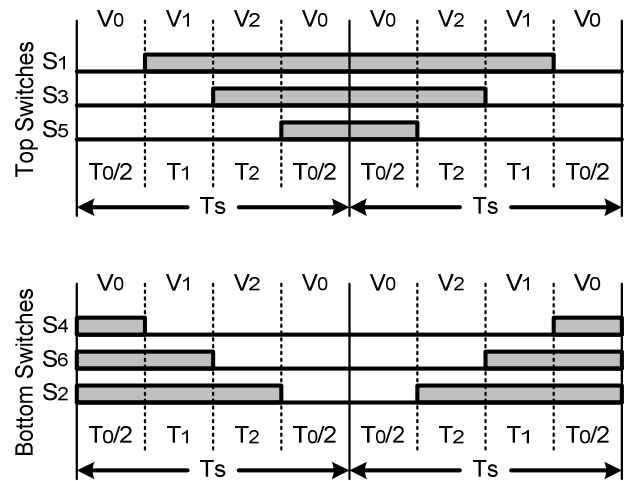


Fig-6: Switching sequence for V_S in sector-1

As shown in the figure (6) the switching sequence is 8,1,2,7 and 7,1,2,8. Here we start and end with the switching sequence [---] so that no switching are required when we move from one sector to next sector.

In the adjacent sector we move in an opposite direction to that of previous sector to ensure minimum switching losses when travelling from one vector to another. So the values of T_1, T_2 will be interchanged for adjacent sectors i.e in sectors 1, 3, 5 the values of T_1, T_2 remain same but in sectors 2, 4, 6 values of T_1 and T_2 will be interchanged.

Let T_{ga}, T_{gb}, T_{gc} be the gating pulses given to top switches of the inverters for 3 phases (A,B,C) respectively. Their complimentary signals are given to the corresponding bottom switches.

$$T_{ga} = T_a + T_b + (T_0/2) \tag{19}$$

$$T_{gb} = T_b + (T_0/2) \tag{20}$$

$$T_{gc} = (T_0/2) \tag{21}$$

These are valid in sector-1. Similarly T_{ga} , T_{gb} , T_{gc} for other sectors can be computed.

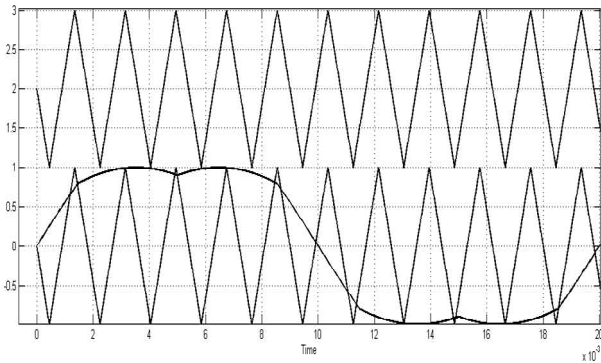


Fig-7: SVPWM for Cascaded Three-level Inverter

4. RESULTS AND DISCUSSIONS

The cascaded three level inverter scheme shown in Fig-1 is simulated using MATLAB/Simulink tool. Two PWM schemes namely Sine-triangle PWM scheme and Space-vector PWM schemes have been used in this paper as a comparative study.

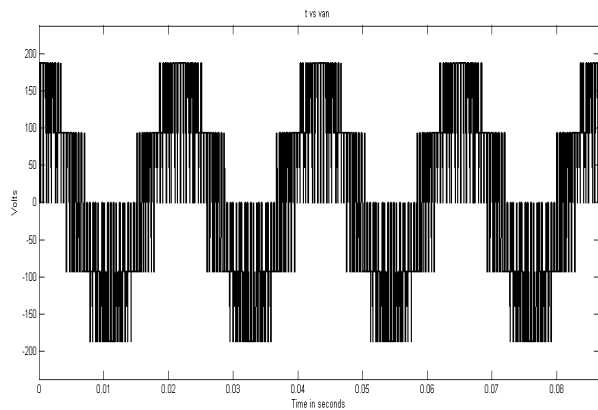


Fig-8: Motor phase voltage for ma=0.4

The simulation results of the SVPWM are presented and the result of sine-triangle PWM scheme is excluded in this paper for simplicity. Fig-8 and Fig-9 shows the motor phase voltage and the motor current waveforms for modulation index of 0.4. Similarly Fig-10 and Fig-11 depicts the phase voltage and currents waveforms for modulation index of 0.7 and Fig-12 and Fig-13 shows the waveforms corresponding to over modulation.

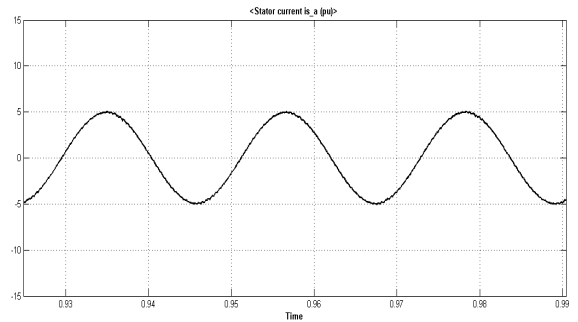


Fig-9: Motor current for ma=0.4

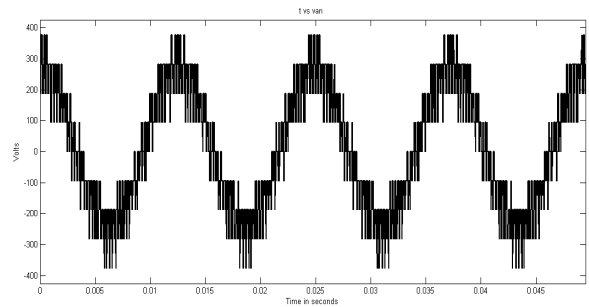


Fig-10: Motor phase voltage for ma=0.7

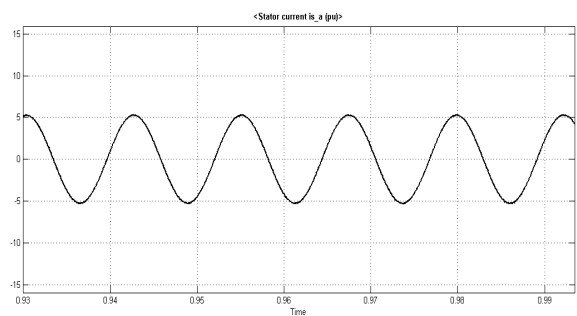


Fig-11: Motor current for ma=0.7

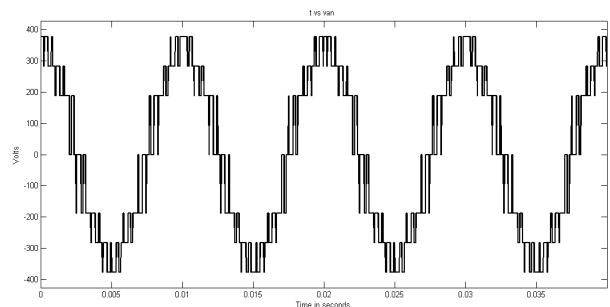


Fig-12: Motor phase voltage for ma=1

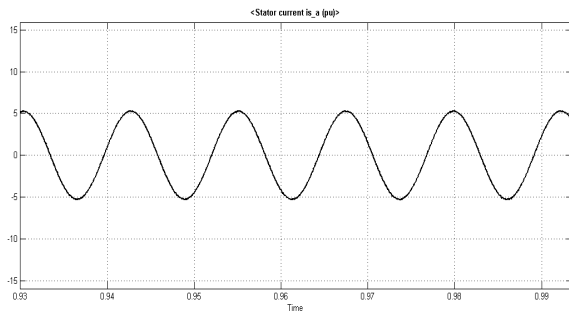


Fig-13: Motor current for $m_a=1$

CONCLUSIONS

In this paper, a space vector based PWM scheme is compared with sine-triangle PWM scheme for a cascaded three-level inverter. From the results it is observed that the sinusoidal pulse width modulation gives a value of $0.612 \cdot V_{dc}$ but using SVM it is observed that the maximum output obtained is $0.707 V_{dc}$ which is 15% higher. So there is a better utilization of DC bus using Space vector modulation PWM scheme. Also SVM offers better harmonic spectrum. Thus this scheme is better than sine-triangle PWM scheme.

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BIOGRAPHIES:



Chunduri Sreeharsha was born in Hyderabad in 1993 and currently he is doing his final year Bachelors in Electrical Engineering at National Institute of Technology, Warangal, Andhra Pradesh, India. His area of interests is Multilevel Inverters.



Inverters.

Anurag Das was born in Kharagpur in 1991 and is pursuing his Bachelors degree and currently in final year in Electrical Engineering at National Institute of Technology, Warangal, Andhra Pradesh, India. His area of interests is Multilevel



Technology, Warangal, India.

Srinivasan Pradabane received his B.Tech degree in from Pondicherry University in 2005 and M.E. from Anna University in 2008. Currently, he is pursuing his PhD degree and is with the Faculty of Electrical Engineering, National Institute of