# COMPARISON OF SYMMETRICAL AND ASYMMETRICAL CASCADED CURRENT SOURCE MULTILEVEL INVERTER

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## Abstract

*This paper presents symmetrical and asymmetrical cascaded multilevel inverter approach for high power output applications. It is based on the cascade connection of the H-bridge inverter cells. Comparison of symmetrical and asymmetrical current source multi level inverter is shown using 2 H-bridge inverter cells with cascade connection. Now ever by the supplies which are in GP with different ratios like 2,3,etc. Structural and operational characteristics are discussed and their inherent advantages are shown. Simulation using Matlab Simulink is done to verify the performance. Simulation and results for this proposed scheme are presented in this paper.*

***Index Terms:*** *Asymmetrical cascaded multilevel inverter, Current source multi level inverter, MATLAB Simulink, Optimization angle control, Symmetrical multi level inverter, Total harmonic distortion (THD).*

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## 1. INTRODUCTION

Numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative these new types of inverters are suitable for high voltage/current and high power application due to their ability to synthesize waveforms with better harmonic spectrum. Different types of topologies have been introduced and widely studied for utility and drive applications. Amongst these topologies, the multilevel cascaded inverter was introduced in Static VAR compensation and drive systems.

The multilevel inverter [MLI] is a promising inverter topology for high voltage/current and high power applications. This inverter synthesizes several different levels of DC voltages to produce a staircase (stepped) that approaches the pure sine waveform. It has high power quality waveforms, lower voltage ratings of devices, lower harmonic distortion, higher switching frequency and lower switching losses, higher efficiency, reduction of dv/dt stresses. It gives the possibility of working with low speed semiconductors if its comparison with the two-level inverter. Most popular MLI topologies are Diode Clamp or neutral point clamp, Inductor clamp and Cascaded Multilevel Inverter (CMLI). In this paper we use a CMLI that consist of some H-Bridge inverters and with equal and un-equal DC current sources. Here we have shown comparison between symmetrical cascaded multilevel inverter (SCMLI) and asymmetrical cascaded multilevel inverter (ACMLI). It is implemented because this inverter is more modular and simple in construction and has other advantages than Diode clamp and flying capacitor.

There are many modulation techniques to control this inverter, such as Selected Harmonics Elimination or Optimized Harmonic Stepped-Waveform (OHSW), Space Vector PWM (SVPWM), Carrier-Based PWM (CBPWM), Symmetrical step control, Optimization angle control, Comparison control technique, etc. In this paper we have used optimization angle control technique as an inverter control technique.

The voltage source inverter produces a defined voltage waveform for the load while the current source inverter outputs a defined current waveform. The current source inverter features simple converter topology, motor-friendly waveforms and reliable short-circuit protection. Therefore, it is one of the widely used converter topologies for the medium voltage drive.

## 2. CONTROL TECHNIQUE

Among other modulation optimization angle control strategies are the most popular methods used in CMLI because they are simple, efficient and easy to implement in hardware. In this method for different current levels proper firing angles are calculated from sine equation. According to the optimized firing angles output voltages are obtained.

I= Im Sinωt.

- 4firing angles obtained for π duration in 5 level inverter
- 6 firing angles obtained for π duration in 7 level inverter
- 8 firing angles obtained for π duration in 9 level inverter

The scheme of Optimization angle control technique for CMLI was proposed to improve the output voltage and current waveform with less THD.

## 3. MULTI LEVEL INVERTER

There are two types of multi level inverter according to the current source, symmetrical type multi level inverter and asymmetrical type multi level inverter.

In symmetrical multilevel inverter all H-bridge cells are fed by equal current sources and hence all the arm cells produce similar output current steps. If all the cells are not fed by equal rating current sources the inverter becomes an asymmetrical one. In this inverter the arm cells have different effect on the output current.

The cascaded H-bridge inverter consists of power conversion cells each supplied by an isolated dc source on the dc side, which can be obtained from batteries, fuel cells, etc. The advantage of this topology is that the modulation, control and protection requirements of each bridge are modular. It should be pointed out that, unlike the diode-clamped and flying-inductor topologies isolated dc sources are required for each cell in each phase. Fig. shows a three-phase topology of a cascade inverter with isolated dc-current sources. An output phase-current waveform is obtained by summing the bridges output currents.

$$Io\,(t) = Io_1\,(t) + Io_2\,(t) + \cdots + Io_n\,(t) \quad \ldots\ldots\ldots (1)$$

where $n$ is the number of cascaded bridges.

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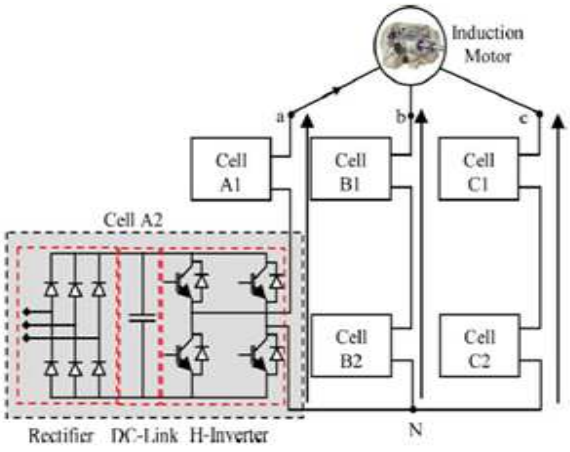



**Fig:** Structure of two cells cascaded multi level inverter

The inverter output voltage $Io\,(t)$ may be determined from the individual cells switching states,

$I_{0\,(t)} = \Sigma(\mu_j - 1)\, I_{dc,}\, j, \qquad \mu_j = 0,1,\ldots.$

If all dc-current sources in Fig. are equal to $I_{dc}$ the inverter is then known as a symmetric multilevel one. The effective number of output current levels $n$ in symmetric multilevel inverter is related to the cells number by,

$$n = 1+2\,N$$

To provide a large number of output levels without increasing the number of bridges asymmetric multilevel inverters can be used. It is proposed to choose the dc-current sources according to a geometric progression with a factor of 2 or 3. For $N$ of such cascade inverters, one can achieve the following distinct current levels

$n = 2N+1 - 1$, if $I$dc,$j = 2j-1I$dc, $j$= 1, 2, . .,$N$ $\quad n = 3N$, if $I_{dc}$,$j = 3j-1I_{dc}$, $j$= 1, 2, . . . , $N$.

Typical waveforms of Fig. multilevel inverter with respectively two dc current sources ($I_{dc}$ and $2I_{dc}$) gives seven-levels output and two dc current sources $I_{dc}$ and $3I_{dc}$ gives nine-level output.

**Table 1** Comparison of multilevel inverter

| | Symmetrical Inverter | Asymmetrical Inverter | |
|---|---|---|---|
| | | Binary | Ternaary |
| N | 2N+1 | $2^{N+1}$ | $3^N$ |
| DC source number | N | N | N |
| Switches number | 4N | 4N | 4N |
| $V_{0MAX(pu)}$ | N | $2^N$-1 | $(3^N-1)/2$ |

The maximum output current of these $N$ cascaded multilevel inverters is

$I_{o,\,MAX} = \Sigma\, I_{dc}$ , j.

Equation can be re written as,

$I_{o,\,MAX} = (2^N - 1)\, I_{dc}.$ If $I_{dc,j} = 2^{j-1}\, I_{dc,}$ j= 1, 2,……, N

$I_{o,\,MAX} = ((2^N - 1)/2)\, I_{dc}.$ If $I_{dc,j} = 3^{j-1}\, I_{dc,}$ j= 1, 2,……, N

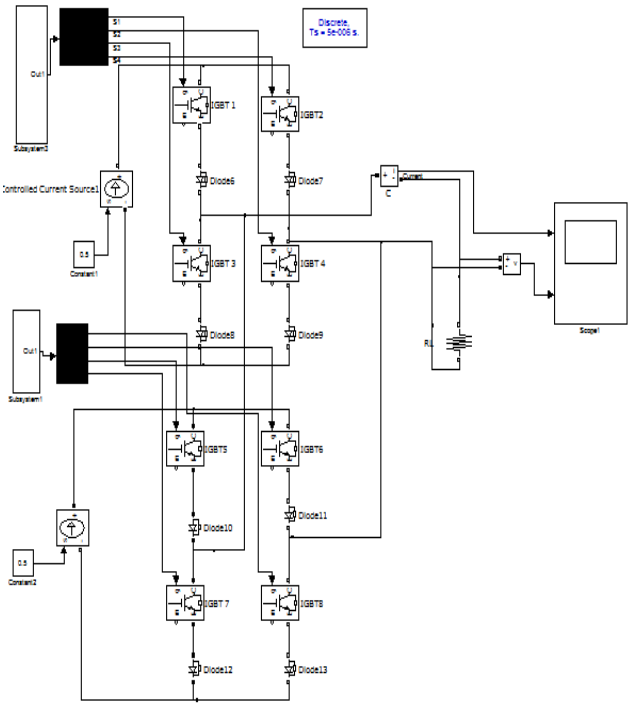
In ACMLI DC current with ratio binary (2) and ternary (3) are the most popular. In binary progression within H-Bridge inverters, the DC current having ratio 1: 2: 4: 8. . : 2N and the maximum current output would be $(2^N$-1) I dc and the current levels will be $(2^{N+1}$-1). While in the ternary progression the amplitude of DC currents having ratio 1: 3: 9: 27. . : 3N and

the maximum output currents reaches to $((3^N - 1)/2)$ I dc and the current levels will be $(3^N)$. Comparing the equations it can be seen that asymmetrical multilevel inverters can generate more current levels and higher maximum output voltages with the same number of bridges.

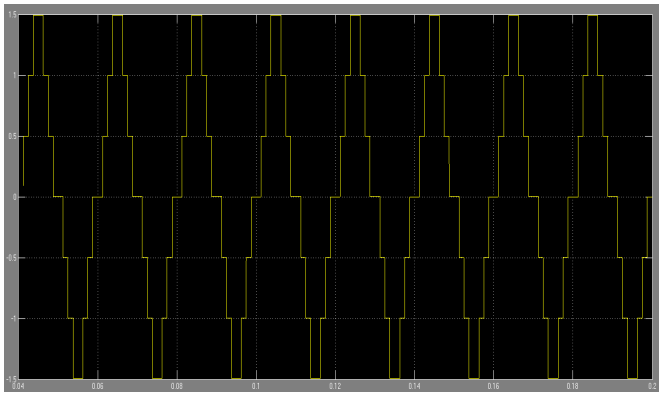
Table summarizes the number of levels, switches, dc sources and maximum available output for classical cascaded multilevel inverters. Increasing the number of levels provides more steps and hence the output current will be of higher resolution and the reference sinusoidal output current can be better achieved.

## 4. SIMULATION AND SIMULATION RESULTS:

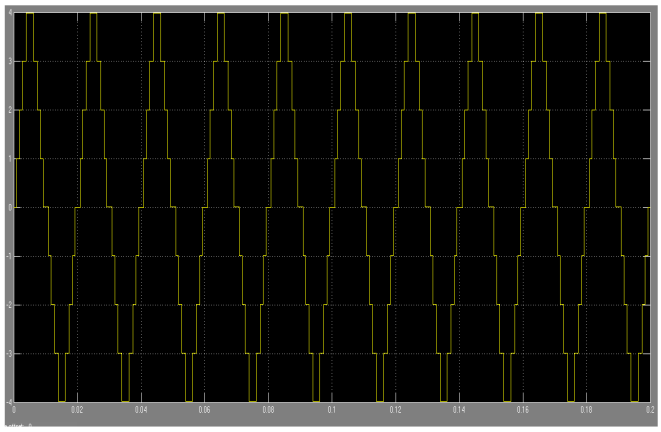
To show the comparison of SCMLI and ACMLI simulation model is used with two bridges. In SCMLI with using two bridges 5 level of output current is achieved while in ACMLI with binary GP ratio we can obtained 7 level of output current and with using ternary GP ratio we can get 9 level output current With using same no of components we can obtained different output current levels but with different THD magnitudes. The output results with same no of bridges but with different sources are shown below.




Output of SCMLI using two bridges



Output of ACMLI using two bridges with binary GP ratio



Output of ACMLI using two bridges with ternary GP ratio

The THD result is summarized below obtained from the above output waveforms of the currents.

**TABLE 2**

| Types Of Multi Level Inverter | NO. Of Bridges | NO. of Current Levels | THD(%)With Optimum Angle Method |
|---|---|---|---|
| SCMLI | 2 | 5 | 20.85 |
| ACMLI with Binary ratio | 2 | 7 | 14.73 |
| ACMLI with Ternary ratio | 2 | 9 | 14.11 |

The above results show that as we increase the no of output levels THD reduces. For that if we want to increase the output current level to reduced the THD level using SCMLI, we have to increase the no of bridges. Hence the cost will increase compared to ACMLI. For obtaining same no of output level SCMLI is costly than the ACMLI. But symmetrical type multi level inverter it is easy to control compared to ACMLI. SCMLI requires equal rating sources while in ACMLI the rating of sources are different and must be kept according to GP ratio.THD for same no of bridges in ACMLI is less compared to SCMLI is less and hence ACMLI is efficient than SCMLI.

## CONCLUSIONS

The scheme of Optimization angle control technique for CMLI was proposed to improve the output current. And it has been concluded that by increasing no. of levels for the output current, the THD can be reduced. No. of levels can be increased by increasing the no. of bridges of MLI. Further for same no. of bridges in ACMLI, in ternary progression output current has more levels then binary . ACMLI are cheaper than the SCMLI and also operate at low THD levels with same no of bridges. Due to its inherent advantages ACMLI is most preferable than SCMLI.

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