A NEW CASCADED MULTILEVEL INVERTER WITH LESS NO OF SWITCHES

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Abstract

In this paper proposed a new topology for cascaded multi level inverters. This structure consists of series connection of proposed basic unit blocks which are built with both unidirectional and bidirectional switches. The proposed structure has some advantages including: reduction in the number of switches and driver circuits, cost and installation area. Three algorithms for determination of dc voltages sources' magnitudes have also been proposed. The algorithms can produce all odd and even levels at the output voltage the proposed structure also has fewer dc voltage sources variety and less maximum blocking voltage of switches compared to conventional inverters. The capability of proposed structure This paper propose a new topology for cascaded multilevel in producing all odd and even output voltage levels is proved by simulation result for a 21-level inverter.

Keywords*: Multilevel inverters, symmetric multilevel, asymmetric multilevel*

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1. INTRODUCTION

Nowadays, multilevel inverters have become more attractive for their use in high-voltage and high-power applications. In multilevel inverters, the desired output voltage is achieved by suitable combination of multiple low dc voltage sources used at the input side. As the number of dc sources is increased, the output voltage becomes closer to a pure sinusoidal waveform. The required dc voltage can be chosen from different sources such as batteries, photovoltaic, fuel cells, capacitors, the rectified output voltage of wind turbines, and other similar dc voltage sources [1-3]. Some advantages of multilevel inverters are good power quality, low switching losses and electromagnetic compatibility due to the low dv/dt transitions [4].

Some of the fundamental multilevel topologies include the cascaded H-bridge structures [5], flying capacitor [6], and diode-clamped converter [7]. Other proposed configurations for multilevel converters are mainly derived from these three basic topologies [2], [4], [8-9]. Among these three topologies, cascaded multilevel converter has got more attention in literatures [10-11]. This paper particularly focuses on Cascaded multilevel converters. This topology is divided into two symmetrical and asymmetrical structures. If all dc voltage sources are equal, the inverter is then known as symmetrical multilevel inverter, otherwise it is known as asymmetrical multilevel inverter. In asymmetrical multilevel inverters, the number of produced output voltage levels is high when compared to symmetrical multilevel inverter with the same number of dc voltage sources and switches [12]. One of the main challenges in multilevel inverters is to reduce the number of power electronic switches while considering operational conditions. Although low voltage rate switches can be utilized in a multilevel inverter, each switch requires related deriver circuits. This may cause the overall circuit to be more expensive and complex. So in practical implementation reducing the number of switches and gate deriver circuits are very important.

In recent years, many configurations are presented in order to reduce the number of overall switches used in cascaded multilevel inverters. Some of these structures are in references [4] and [13]. The presented structures aim in reducing the number of switches while having the availability to produce all odd and even levels at the output voltage. The structures presented in these literatures have significant reduction in the number of switches and consequently reduction in installation area. However in the structures of [8] and [13], the implemented switches are bidirectional (consisting of two IGBTs and two anti-parallel diodes). So the total number of IGBTs is high which increases cost. Nevertheless, because of using one deriver circuit for each switch, the overall numbers of deriver circuits needed for the recommended topologies are fewer compared to conventional multilevel inverter.

This paper proposes a new topology for cascaded multilevel inverters which uses a combination of bidirectional and unidirectional switches. It should be considered that by suitable combination of bidirectional and unidirectional switches, fewer deriver circuits and IGBTs can be achieved. Moreover, to produce all odd and even levels at the output voltage, three procedures for determination of dc voltage sources' magnitudes have also been proposed. The capability of proposed structure in producing all odd and even output voltage levels is proved by simulation result for a 21-level inverter.

2. PROPOSED TOPOLOGY

Fig. 1 illustrates basic unit for proposed cascaded multilevel inverter. As shown in Fig.l, the basic unit consists of 2 dc voltage sources and 3 switches. The switches S1 and S3 are unidirectional (consisting of an IGBT with an anti-parallel diode) and switchS2 is bidirectional (consisting of two IGBTs and two anti parallel diodes). It is clear that switches (S1 and S2)' (S2 andS_3) and (S1' S2 and S_3) should not be on simultaneously because a short circuit across dc voltage would be produced. The permitted on and off states for the switches of recommended topology are given in Table 1. As it shown in Table I, the proposed basic unit can produce all three voltage levels (0, and + V;). This structure can only produce positive values of output voltage.

The overall structure can be obtained by the series connection of n basic units. Using this method, total output voltage would be sum of basic units' output voltage. It should be noted that if n basic units are connected in series, then the overall structure can produce all voltage levels. The resulting structure is shown in Fig. 2 which can produce all positive voltage levels. Instantaneous output voltage of proposed in which vo,l (t), vo,2 (t), ... , vo,n (t)are the output voltages of units 1, 2, ..., n, respectively. cascaded multilevel inverter can be evaluated by:

$$V_{0,1}(t)=V_{0,1}(t)+V_{0,2}(t)+V_{0,3}(t)+\text{-----}+V_{0,n}(t) \quad (1)$$

In which V0,1(t),Vo,2(t), ……. Vo,n(t) are output voltages of units 1,2 …..,n respectively

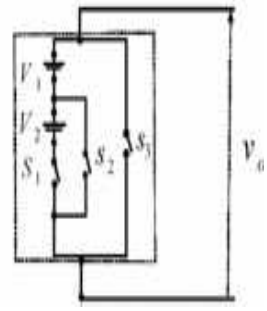


Fig1.Proposed basic unit for a sub-multilevel inverter

Table I. ON AND OFF SWITCHING STATES FOR THE RECOMMENDED STRUCTURE

states	Switches state			V_0
	S_1	S_2	S_3	
1	off	off	on	0
2	off	on	off	V_1
3	on	off	off	V_1+V_2

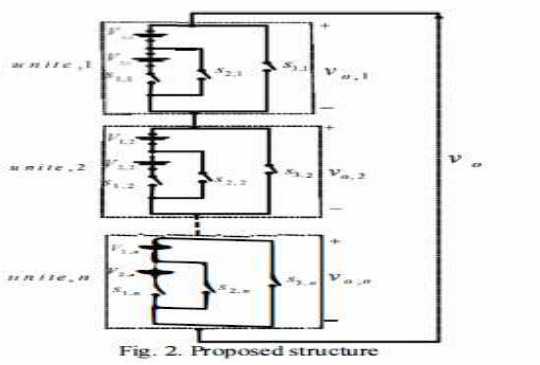


Fig. 2. Proposed structure

The switches $S!_{v,}i_o$ and S . are unidirectional and S .are bidirectional and i=l, 2, ..., n.

Table II shows the different values of for different on and off states of switches.

For the proposed structure, the number of switches (Nswitch)' !GBTs (NIGBT) and dc voltage sources (N $_s$ource) according to the number of utilized units (n) are as follow:

$$N_{switch}= 3n \quad \text{for} \quad n=1,2\ldots.. \quad (2)$$

$$N_{IGBT} = 4n \quad \text{for} \quad n=1,2\ldots.. \quad (3)$$

$$N_{Source}= 2n \quad \text{for} \quad n=1,2\ldots\ldots \quad (4)$$

The number of output voltage levels in the proposed structure depends on dc voltage sources' magnitude. In follow, three algorithms for determination of dc voltage sources' magnitudes are proposed.

Table II. DIFFERENT VALUES OF Vo FOR DIFFERENT ON AND OFF STATES OF SWITCHES

STATES			**1**	**2**	**3**	**…**	n_{step}
Switches states	**Unit 1**	$S_{1,1}$	**Off**	**Off**	**On**		**On**
		$S_{2,1}$	**Off**	**On**	**Off**		**Off**
		$S_{3,1}$	**On**	**Off**	**Off**		**Off**
	Unit 2	$S_{1,2}$	**Off**	**Off**	**Off**		**On**
		$S_{2,2}$	**Off**	**Off**	**Off**		**Off**
		$S_{3,2}$	**On**	**On**	**On**		**Off**
	⋮	⋮	⋮	⋮	⋮	⋯	⋮
	Unit 3	$S_{1,3}$	**Off**	**Off**	**Off**		**On**
		$S_{2,3}$	**Off**	**Off**	**Off**		**Off**
		$S_{3,3}$	**On**	**On**	**On**		**Off**
	⋮	⋮	⋮	⋮	⋮	…	⋮
$V_0(t)$			**0**	$V_{1,1}$	$V_{1,1}+V_{2,1}$	⋯	$\sum_{i=0}^{n}\sum_{K=0}^{2} Vj,k$

A. First Method

In the first algorithm, all dc voltage sources in Fig. 2 are considered to be equal to Vdc •

$$V_{1j}=V_{2j}=V_{dc} \quad \text{for} \quad j=1,2.. \qquad (5)$$

In this method, the number of output voltage levels according to the number of series connected units is:

$$N_{step1} =2n+1 \quad \text{for} \quad n=1,2 \qquad (6)$$

The maximum output voltage is given by:

$$V_{omax1} = 2n \quad \text{for} \quad n=1,2 \qquad (7)$$

One of the important problems in multilevel inverters is the variety of the magnitudes of dc voltage sources. As the variety decreases, the overall structure cost reduces. The variety of dc voltage sources in this algorithm is as follow:

$$N_{variety1}= 1 \qquad (8)$$

Another important problem in inverters is the ratings of switches. In other word, voltage and current ratings of the switches in a multilevel inverter play important roles on the cost and realization of the inverter. In the proposed topology, the currents of all switches are equal with the rated current of the load. This is however not the case for the voltage. As maximum blocking voltage of switches$_3$ reduces, the overall cost decreases [8]. In the recommended topology, the maximum$_{,n}$ blocking voltage of switches in j-th unit is given by following equation:

$$V_{switch,j} = \sum_{K=1}^{3} V_{switch,j,k} \text{ for } j=1,2.. \qquad (9)$$

In above the above equation, Vswitch, $_{j,\ k}$ represents the peak voltage of the switches in stage k. The maximum standing voltage is as follows:

$$V_{switch,1}= \sum_{j=1}^{n} V_{switch,j} \qquad (10)$$

Equation (9) can be considered as a criterion for the comparison of different topologies since smaller value of Vswitch1 results in lower cost. In the first method, the value of can be calculated as follow:

$$Vswitch,1= \sum_{k=1}^{3} Vswitch,j,k = Vswitch,j,1+Vswitch,j,2+ Vswitch,j,3 \qquad (11)$$

$$= (V_{1j}+ V_{2j}) + (V_{2j}) + (V_{1j}+ V_{2j})$$

According to (10), the maximum blocking voltage is given by (12).

$$V_{switch,1}=n5(Vdc) \qquad (12)$$

B. Second Method

In this method, the dc voltage sources' magnitudes are determined using (13).

$$V_{1,1}=0.5V_{1,j}=V_{2,1}=0.5V_{2,j}=V_{dc} \qquad (13)$$

The number of output voltage steps(Nstep,2)maximum output voltage(V 0 ,max,2) and the variety of dc voltage sources (Nvarity,2) for this method is given by(14) and (15) and (16), respectively.

$$N_{step2} = 4n - 1 \quad \text{for} \quad n=1,2, .. . \qquad (14)$$

$$V_{0,max2} = 4n -2 \quad \text{for } n = 1,2, .. . \qquad (15)$$

$$N_{variety,2} = 2 \qquad (16)$$

According to (l0), the maximum blocking voltage of switches (VsWitch2) for the second method is given by

$$Vswitch,2= (10n-5) Vdc \qquad (17)$$

C. Third Method

In the third method, the dc voltage sources magnitudes are determined using (18).

$$V_{1,j} = V_{2j} = 2^{j-1}V_{dc} \qquad (18)$$

The number of output voltage steps(N,step,3) maximum output voltage (V0,max,3) and the variety of dc voltage sources (Nvarity,3) for this method is given by (19)-(21)respectively

$$N_{step3} = 2^{n+1} - 1 \quad \text{for} \quad n=1,2, .. . \qquad (19)$$

$$V_{0,max3} = 2^{n+1}-2 \quad \text{for } n = 1,2, .. . \qquad (20)$$

$$N_{varity,3} = n+1 \qquad (21)$$

According to (10) the maximum blocking voltage is given by(22)

$$V_{switch3} = (10x2^{n-1}-5)\ V_{dc} \qquad (22)$$

Since the dc voltage sources' magnitudes in first and second methods are not equal, the resulting multilevel converter would be asymmetrical. As expected, in asymmetrical multilevel converters, the number of voltage steps and maximum output voltage for the same number of sources and

switches are more when compared to symmetrical multilevel converters.

3. PROPOSED EXTENDED STRUCTURE

The multilevel proposed in Fig. 2, only can generate the positive output voltages. For generating both of the positive and negative output voltages, the structure shown in Fig. 3 is proposed. In this figure, the full bridge topology with four switches (T1,T4)are added to the output terminals of the circuit shown in Fig. 2. It is clear that switches on a leg can not be on simultaneously because a short circuit across the voltage would be produced. To produce positive half of output voltage the switches T1and T4 and for the negative half, T;, and T; should be fired together. It worth to note that the switches used in H-bridge inverter at the load terminal, must be able to block the entire dc voltage source used the recommended structure. The entire blocking voltage by H-bridge switches can be calculated using (23).

$$N_{switch,H} = 4\left(\sum_{j=1}^{n}\sum_{k=1}^{3} V_{k,j}\right) \quad (23)$$

The above equations confirm that four high rated voltages for the proposed structure are needed. The numbers of switches and IGSTs for recommended structure are given as follows

$$N_{switch} = 3n+4 \quad \text{for } n=1,2\ldots \quad (24)$$

$$N_{IGBT} = 4n+n \quad \text{for } n=1,2\ldots \quad (25)$$

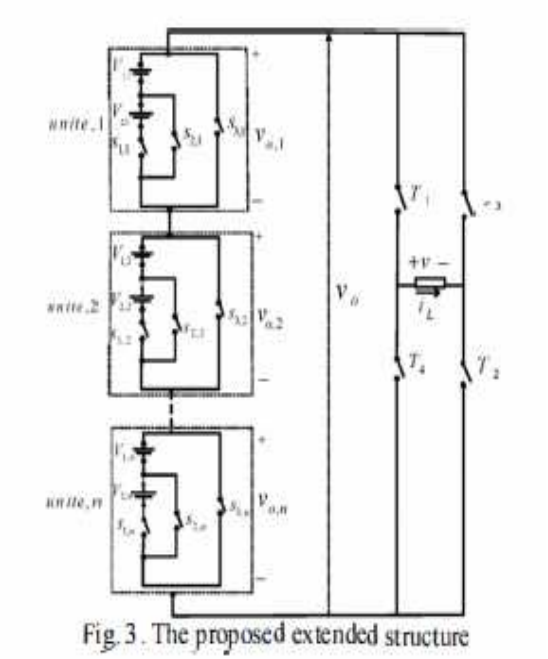


Fig. 3. The proposed extended structure

The no of voltage steps for three algorithms can be calculated using (26)-(28),respectively.

$$N_{step,1} = 4n+1 \quad \text{for } n=1,2.. \quad (26)$$

$$N_{step,2} = 8n-3 \quad \text{for } n=1,2.. \quad (27)$$

$$N_{step,3} = 2^{n+2}-3 \quad \text{for } n=1,2\ .. \quad (28)$$

3. COMPARISON OF THE PROPOSED STRUCTURE WITH CONVENTIONAL CASCADED MULTILEVEL INVERTER

The main purpose of this paper is reduction of the components of the cascaded multilevel inverters. As mentioned in previous section, the proposed structure is a combination of bidirectional and unidirectional switches. Since each switch needs only one deriver circuit, the overall number of deriver circuits is equal to the number of switches (Ndrive,) .

In Table III, different parameters of proposed structure concerning the number of voltage steps in the three algorithms are summarized

Table III. DIFFERENT PARAMETERS OF PROPOSED STRUCTURE CONCERNING THE NUMBER OF VOLTAGE STEPS

	First Proposed Algorithm	Second Proposed Algorithm	Third Proposed Algorithm
$V_{0,max}$	$\frac{1}{2}(N_{step}-1)V_{dc}$	$\frac{1}{2}(N_{step}-1)V_{dc}$	$\frac{1}{2}(N_{step}-1)V_{dc}$
N_{switch}	$\frac{3Nstep+13}{4}$	$\frac{3Nstep+32}{8}$	$3\ln\left(\frac{\frac{Nstep+3}{4}}{\ln 2}\right)+4$
N_{IGBT}	Nstep +3	$\frac{Nstep+11}{2}$	$4x\left(\frac{\ln(Nstep+3)}{\ln 2}-1\right)$
N_{driver}	$\frac{3Nstep+13}{4}$	$\frac{3Nstep+32}{8}$	$\frac{2\ln\left(\frac{Nstep+3}{4}\right)}{\ln 2}$
N_{varity}	1	2	$\ln\left(\frac{\frac{Nstep+3}{2}}{\ln 2}\right)$
V_{switch}	$\frac{(5Nstep-5)Vdc}{4}$	$(N_{step})XV_d$	$(10X2^{\frac{\ln(Nstep+3)}{\ln 2}}-5)Vdc$

For highlighting sufficiency of proposed structure, different parameters of recommended structure for the same conditions are compared to that presented in [4] (Fig. 4(a), [13] (Fig. 4(b) and conventional cascaded multilevel converters (Fig4(c). It is noteworthy that switches used in reference [13] are bidirectional. Although, two IGBTs are used in bidirectional switches, in case of using common emitter configuration,

onecircuit deriver can be used for them [2]. The dc voltage source magnitudes of [4] and [13] and conventional cascade converter must be selected in a way which all odd and even voltage steps can be produced. For this purpose, for the structure offered in [4], two method including symmetrical (all dc voltage sources are equal) and binary (in which the magnitude of dc sources are selected as a power of 2) is used. Likewise, for the structure offered in [13], only one state can be considered in which all dc voltage sources are set to be equal. Also for the conventional cascaded multilevel inverter three algorithms (symmetrical, binary and tri nary) can be considered. The results of comparison for the recommended configuration and pre-mentioned structures are investigated. Fig. 5 compares the recommended configuration with the structures recommended in [4] and [13] and conventional cascaded multilevel inverter concerning the number of switches, number of IGBTs, number of deriver circuits, number of dc voltage sources, variety of sources and maximum standing voltage for symmetrical and asymmetrical structures.

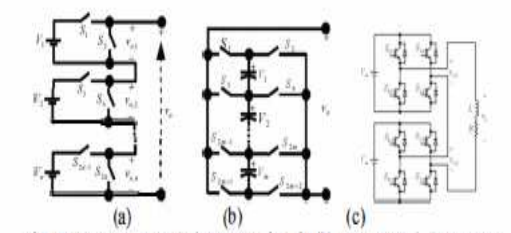
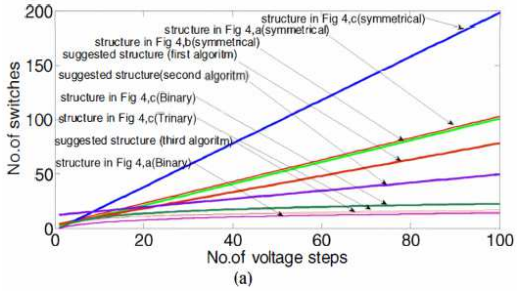
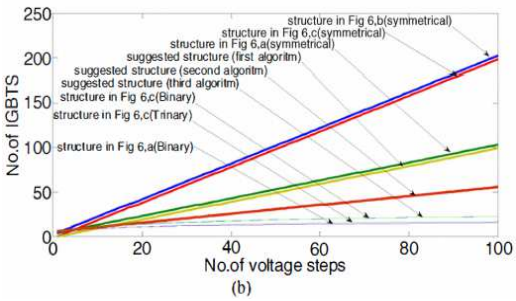
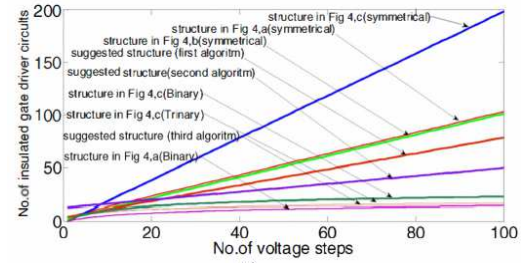
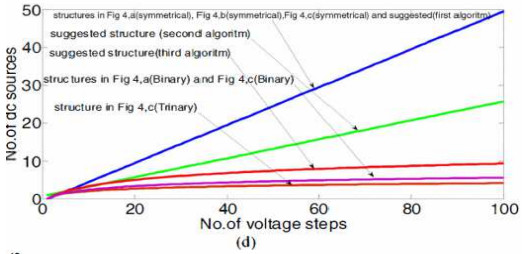


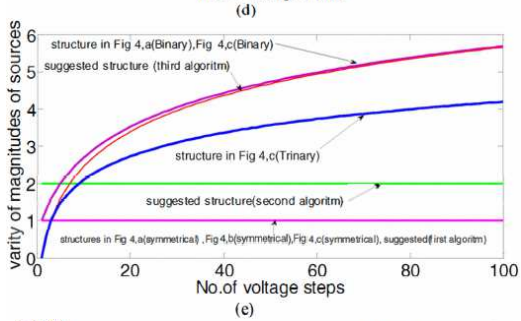
Fig. 4. (a) Recommended structure in [4]; (b) recommended structure in [13]; (c) conventional cascaded inverter

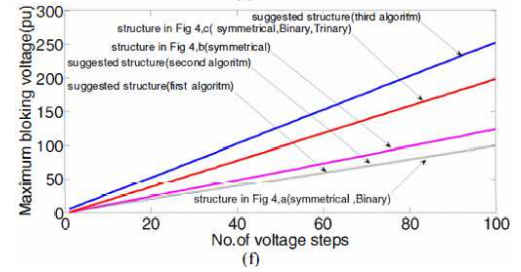












From Fig. 5(a), it can be seen that the number of switches used in proposed structure, are less than in comparison with the conventional structures Fig. 5(b)confirms that for symmetrical mode, the proposed structure needs fewer IGBTs in comparison with other three structures. Similar results can be obtained for the number of deriver circuits as shown in Fig. 5(c). As shown in Fig. 5(d), the number of sources used in all structures (symmetrical) is the same. Another important problem in multilevel inverters is the variety of the magnitudes of dc voltage sources. As the variety decreases, the overall structure cost reduces. According to Fig. 5(e), in symmetrical mode, the variety of the magnitudes of dc voltage sources are the same for all structures. According to Fig. 5(e), the results of comparison reveal that the proposed topology has less variety in asymmetrical mode. Fig. 5(t) illustrates another important parameter named standing voltage across switches for all structures.

5. SIMULATION RESULTS

To examine the performance of proposed multilevel inverter in generation of a desired output voltage waveform, a 21-level inverter based on proposed topology as shown in Fig. 6 is simulated in MATLABSIMULINK environment. It should be mentioned that the magnitude of structure in Fig. 6 is chosen based on second algorithm. This inverter can generate staircase output voltage waveform with maximum of 200V. The load is a series R-L with magnitudes R = 70Q and L = 55mH , respectively. There are several modulation strategies [8, 13]. In this work, the fundamental frequency switching technique has been used. Table IV shows the switching pattern of structure in Fig. 6 to produce different output voltage levels. Fig. 7 shows the control block diagram of inverter. The main idea in control strategy is to deliver the load a voltage that minimizes the error with respect to reference voltage.

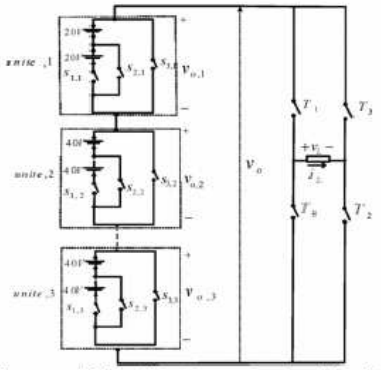


Fig. 6. Structure of 21-level based on proposed multilevel inverter

Table IV. SWITCHING PATTERN TO PRODUCE DIFFERENT OUTPUT VOLTAGE LEVELS

$v_L[pu]$ 20V=1pu	-10	…	-1	0	1	…	10
$S_{1,1}$	on	…	off	off	off	…	on
$S_{2,1}$	off	…	on	off	on	…	off
$S_{3,1}$	off	…	off	on	off	…	off
$S_{1,2}$	on	…	off	off	off	…	on
$S_{2,2}$	off	…	off	off	off	…	off
$S_{3,2}$	off	…	on	on	on	…	off
$S_{1,3}$	on	…	off	off	off	…	on
$S_{2,3}$	off	…	off	off	off	…	off
$S_{3,3}$	off	…	on	on	on	…	off
T_1	off	…	off	on	on	…	on
T_2	off	…	off	off	on	…	on
T_3	on	…	on	on	off	…	off
T_4	on	…	on	off	off	…	off

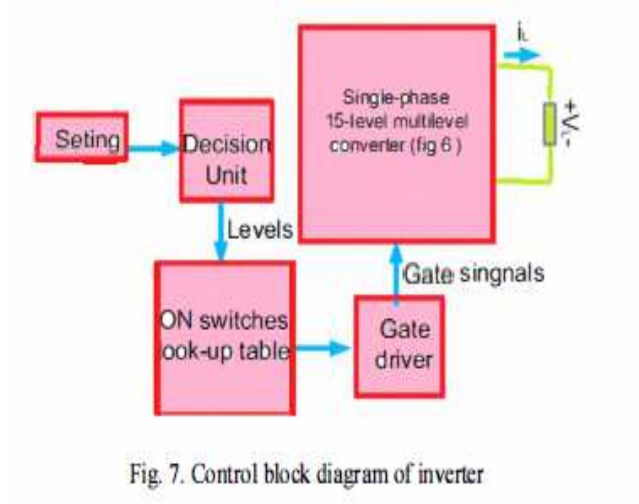


Fig. 7. Control block diagram of inverter

Figures 8 -11 shows the output voltage of different parts in structure. As these figures clearly show, the output voltage of each unit can only produce zero or positive values. By adding H-bridge inverter at the output terminal of circuit shown in Fig. 2, it's possible to produce negative value of output voltage. For the simulated 21-level inverter, the voltage waveforms of load voltage and current are shown in Figs. 12 and 13. From Fig. 13, it's clear that the proposed structure can produce both positive and negative values of output voltage.

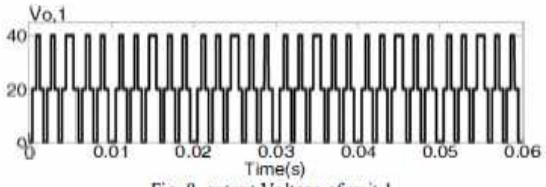


Fig. 8. output Voltage of unit 1

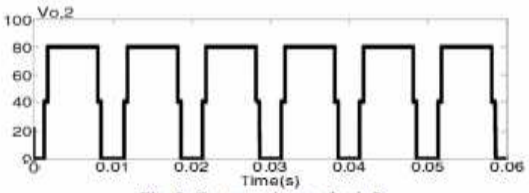


Fig. 9. Output voltage of unit 2

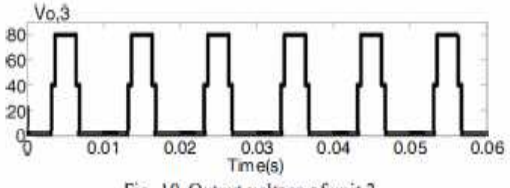


Fig. 10. Output voltage of unit 3

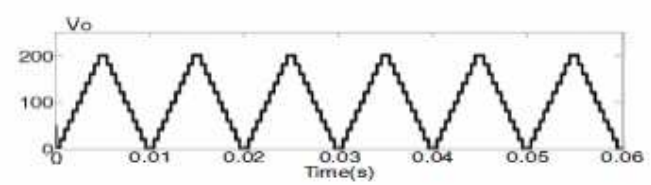


Fig.11. Output voltage v_o

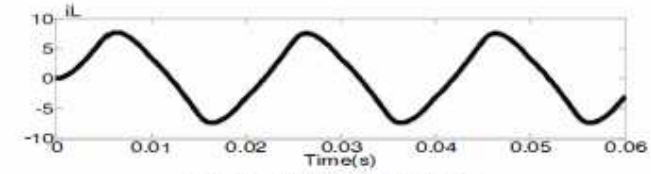


Fig. 12. Load voltage current

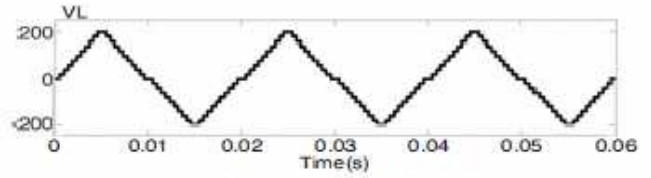


Fig. 13. Load voltage

CONCLUSIONS

In this paper, a new topology has been introduced for cascaded multilevel inverters. The proposed structure is a compound of both bidirectional and unidirectional switches which has the advantage of using fewer IGBTs and deriver circuits. Therefore the proposed topology results in reduction of installation area and cost. Also three procedures have been presented for the determination of dc voltage sources' magnitude. Using these algorithms, both symmetrical and asymmetrical configuration has been made for sources of studied structures and by concerning different points of view including the number of IGBTs, deriver circuit, the variety of dc voltage magnitudes, a comparison has been made between the proposed topology and other referred three structures. The results of the simulation for proposed 2I-level inverter demonstrate that the proposed configuration has prominent feature compared to other cascaded multilevel inverters.

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