OPTIMIZED STUDY OF ONE-BIT COMPARATOR USING REVERSIBLE LOGIC GATES

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Abstract

In digital electronics, the power dissipation is the major problem. So that the reversible gate can be implemented in microelectronics and electronics which have low power dissipation in the digital designing because, in the reversible state in reversible logic it will use no energy. Hence reversible logic has ability to reduce the power dissipation in digital designing. In the Reversible logic, reversibility have a special condition which is reversible computing and reversible computing is based on the principle of BIJECTION DEVICE with a same no. of input and output which means one to one mapping. Reversible logic has numerous applications in the field of electronics and microelectronics which are ultra low power in nanoscale computing, quantum computing, emerging nanotechnology cellular automata and the other approach of reversible logic is ballistic computation, mechanical computation which are the basic technology. This paper presents an optimization of reversible comparator using the existing reversible gates and proposed new Reversible one bit comparator using BVF gate. A comparative result is presented in terms of number of gates, number of garbage outputs, number of constant inputs and Quantum cost.

Keywords— *advanced computing, Reversible logic circuits, reversible logic gates and comparator.*

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1. INTRODUCTION

This reversible circuits (gates) that have one to-one mapping between vectors of inputs and outputs; thus the vector of input states can be always reconstructed from the vector of output states. Rolf Landauer, 1961. Whenever we use a logically irreversible gate we dissipate energy into the environment. The loss of information is associated with laws of physics requiring that one bit of information lost dissipates k T ln 2 of energy, where k is Boltzmann' constant and T is the temperature of the system. Interest in reversible computation arises from the desire to reduce heat dissipation, thereby allowing [1]:

I. higher densities
II. higher speed

Later Bennett, in 1973, showed that these KTln2 joules of Energy dissipation in a circuit can be avoided if it is constructed using reversible logic circuits. A reversible logic gate is an n-input, n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs but also the inputs can be uniquely recovered from the outputs.

Specifically, the fundamentals of reversible computing are based on the relationship between entropy, heat transfer between molecules in a system, the probability of a quantum particle occupying a particular state at any given time, and the quantum electrodynamics between electrons when they are in close proximity. One of the emerging applications of reversible logic is in quantum computers [3, 4]. A quantum computer consists of quantum logic gates. The quantum logic gates perform elementary unitary operation on one, two or more two–state quantum systems called qubits. In quantum computing qubit represents the elementary unit of information corresponding to the classical bit values 0 and 1. Any unitary operation is reversible in nature and hence quantum computers must be built from reversible logical components.

An important constraint present on the design of a reversible logic circuit using reversible logic gate is that fan-out is not allowed. A reversible circuit should be designed using minimum number of reversible gates. One key requirement to achieve optimization is that the designed circuit must produce minimum number of garbage outputs; also they must use minimum number of constant inputs[2].

2. BASIC REVERSIBLE GATES

If mapping in each input pattern to a unique output pattern is taken then the digital combinational logic circuit is reversible. There are many types of reversible gates including: Feynman, Toffoli, Fredkin, Peres, TR, BJN and BVF etc. These gates are defined as follows-

A. Feynman Gate (CNOT gate)

This gate is widely used for fan-out purposes. This Gate is 2*2 gate that means two to two mapping. This Feynman gate is

also called as Controlled NOT and the input of this gate is A&B and output are P=A, Q= A ⊕B as shown in figure. It has Quantum cost one. The gate representation and circuit representation of Feynman gate is shown in below-

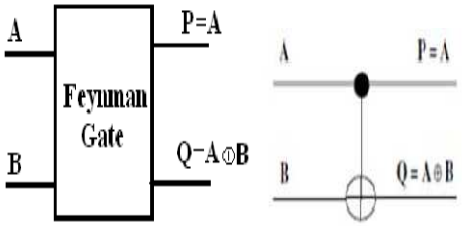


Fig. 1 Feynman Gate [5]

B. Double Feynman Gate (F2G)

This gate is also used in fan-out purposes. Double Feynman is a 3*3 gate in which three input vector is I (A, B, C) and the three output vector is O (P, Q, R) and the outputs are defined by P = A, Q=A⊕B, R=A⊕C. The Quantum cost of double Feynman gate is 2.

The gate representation and circuit representation of double Feynman gate is shown in below-

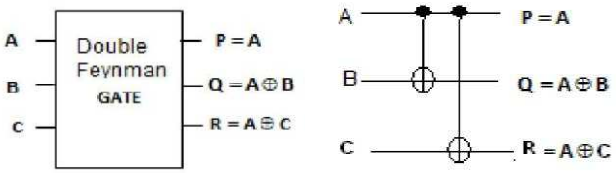


Fig.2 double feynman Gate

C. Toffoli Gate

The Toffoli gate is one of the most popular reversible gates and has quantum cost of 5.Toffoli gate is a 3*3 gate in which three input vector is I (A, B, C) and the three output vector is O (P, Q, R) and output is P=A, Q=B, R=AB⊕C.

The circuit representation and gate representation of Toffoli gate is shown in fig.

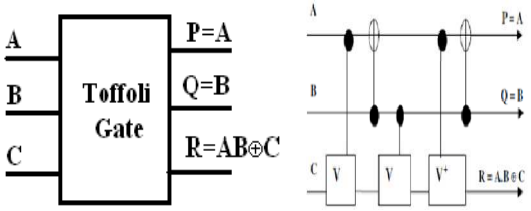


Fig.3 Toffoli Gate[3]

D. Fredkin Gate

Fredkin gate is a conservative reversible gate which have quantum cost 5. Fredkin gate is a 3*3 gate in which three input vector is I (A, B, C) and the three output vector is O (P, Q, R). The output is defined by P=A, Q=A′B ⊕AC and R=A′C⊕ AB. The circuit representation and gate representation of Fredkin gate is shown in fig.

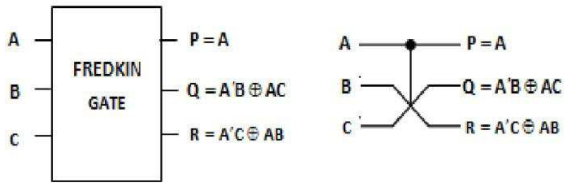


Fig.4 Fredkin Gate [4]

E. Peres Gate

In the existing literature, among the 3*3 reversible gate, Peres gate has the minimum quantum cost and its quantum cost is 4. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = A⊕B and R=AB⊕ C. The circuit representation and gate representation of Peres gate is shown in fig.

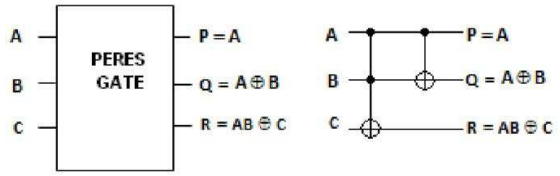


Fig. 5 Peres Gate [6]

F. TR Gate

TR gate is another important gate which has a low quantum cost. .TR GATE is a 3*3 gate in which three input vector is I (A, B, C) and the three output vector is O (P, Q, R) and output is P=A, Q=A⊕B, R = AB'⊕C. The Quantum cost of TR gate is 4.

The circuit representation and gate representation of TR gate is shown in fig.

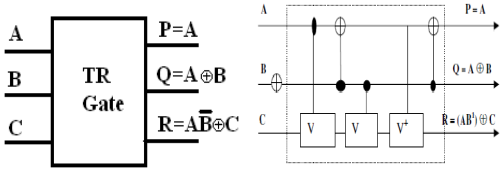


Fig. 6 TR Gate

G. BJN Gate

BJN gate is a 3*3 gate with inputs (A, B, C) and outputs P=A, Q=B, R =(A+B) ⊕C. Its quantum realization is shown in figure. It has quantum cost of 5.

The circuit representation and gate representation of BJN gate is shown in fig.

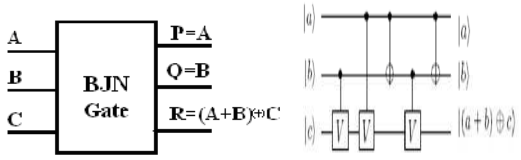


Fig. 7 BJN Gate

H. BVF Gate

BVF gate is a 4*4 gate in which four input vector is I (A, B, C, D) and the four output vector is O (P, Q, R, S) and output is P=A, Q=A⊕B, R=C, S=C⊕D.The Quantum cost of BVF gate is 2.

The gate representation of BVF gate is shown in fig.

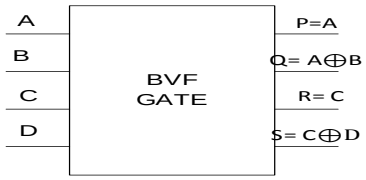
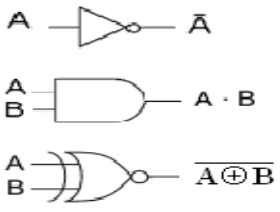


Fig.8 BVF Gate

3. DESIGN OF ONE - BIT COMPARATOR

3.1 Irreversible One-bit Comparator Implementation

For the Implementation of One-bit Irreversible Comparator, we require NOT gates, NAND gate, and XOR gate and these gate is shown in Fig.



From these irreversible gates, we can get the following logic expressions

$$F_{A>B} = A\,\overline{B}$$

$$F_{A<B} = \overline{A}B$$

$$F_{A=B} = \overline{A \oplus B}$$

In the proposed one-bit comparator design, we have considered FA>B and FA=B and the third condition FA<B is generated from the first two outputs. Hence the design expression leads to

$$F_{A>B} = A\,\overline{B}$$

$$F_{A=B} = \overline{A \oplus B}$$

$$F_{A<B} = A \oplus B \oplus A\,\overline{B} = \overline{A}B$$

4. ONE-BIT REVERSIBLE COMPARATOR DESIGN

A. Conventional reversible logic

1. One- bit comparator using Peres and BJN gate

Reversible one bit comparator is implemented with Feynman gate and Peres gate and BJN gate as shown in fig. The number of garbage outputs is two and represented as G1 and G2, it uses three constant inputs one logic ‘0’ and two logic ‘1’ and its quantum cost is 10.

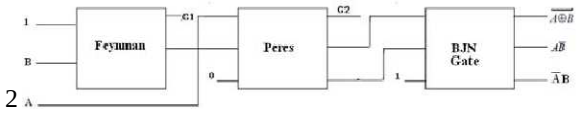


Fig. 9 one bit comparator using Peres gate

a. Proposed Reversible Logic

1. One- bit comparator using Peres and BVF gate

Reversible one bit comparator is implemented with DFG gate and Peres gate and BVF gate as shown in fig. The numbers of garbage outputs are two and represented as G1 and G2, it uses two constant inputs one logic ‘0’ and two logic ‘1’ and its quantum cost is 8.

Fig.10 Proposed one bit comparator using Peres gate

B. Conventional reversible logic

1. One bit comparator using Toffoli and BJN gate

Reversible one bit comparator is implemented with Feynman gate and Toffoli gate as shown in fig. The number of garbage outputs are two and represented as G1 and G2, it uses three constant inputs, one logic '0' and two logic '1' it requires one Feynman gate and two Toffoli gates and its quantum cost is 16.

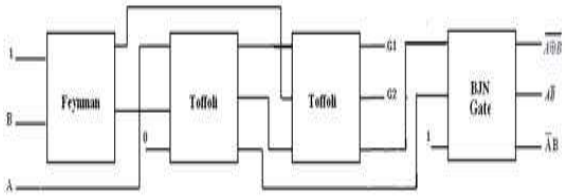


Fig.11 one bit comparator using Toffoli gate

b. Proposed Reversible Logic

1. One bit comparator using Toffoli and BVF gate

Reversible one bit comparator is implemented with DFG gate and Toffoli gate and BVF gate as shown in fig. The number of garbage outputs are two and represented as G1 and G2, it uses two constant inputs, one logic '0' and two logic '1' and its quantum cost is 9.

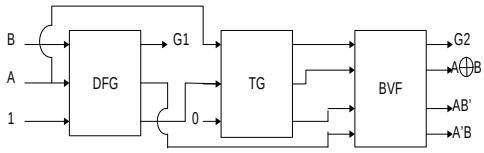


Fig .12 Proposed one bit comparator using Toffoli gate

C. Conventional reversible logic

1. One bit comparator using Fredkin and BJN gate

Reversible one bit comparator is implemented with Feynman gate and Fredkin gate and BJN gate is as shown in fig. The number of garbage outputs are six and represented with G1 to G6, it uses seven constant inputs, four logic '0' and three logic '1' and its quantum cost is 23.

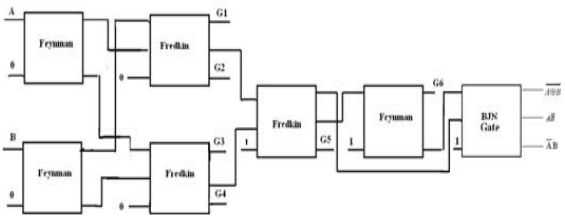


Fig. 13 one bit comparator using Fredkin gate

c. Proposed Reversible Logic

1. One bit comparator using Fredkin and BVF gate

Reversible one bit comparator is implemented with BVF gate and Fredkin gate and BVF gate is as shown in fig. The number of garbage outputs is three and represented with G1 to G3, it uses two constant inputs, logic '0' and logic '1' and its quantum cost is 9.

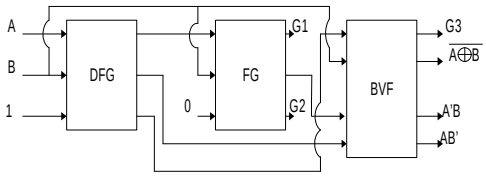


Fig. 14 Proposed one bit comparator using Fredkin gate

D. Conventional reversible logic

1. one bit comparator using TR and BJN gate

Reversible one bit comparator is implemented with Feynman gate and TR gate and BJN gate as shown in fig. The number of garbage outputs are two and represented with G1 and G2, it uses three constant inputs, one logic '0' and two logic '1' and its quantum cost is 12.

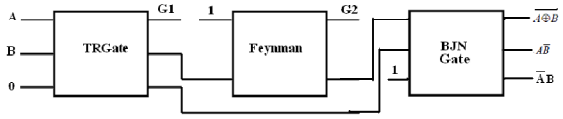


Fig.15 one bit comparator using TR gate

d. Proposed Reversible Logic

1. one bit comparator using TR and BVF gate

Reversible one bit comparator is implemented with Feynman gate and TR gate and BVF gate as shown in fig. The number of garbage outputs are one and represented as G1, it uses two constant inputs, logic '0' and logic '1' and its quantum cost is 7.

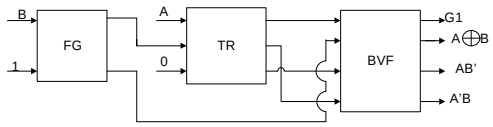


Fig. 16 Proposed one bit comparator using TR gate

5. COMPARISON AND DISCUSSION

The comparison between the conventional one bit comparator and proposed one bit comparator can be done with the help of following parameters-

A. Garbage Outputs:

This refers to the number of outputs which are not used in the synthesis of a given function. These are very essential without which reversibility cannot be achieved.

B. Gate count:

The number of reversible gates used to realize the function.

C. Constant Inputs:

This refers to the constant inputs '0' or '1'.

So that the comparison between the conventional comparator and proposed comparator can be understand with the following table and charts in the terms of garbage output, gate count, constant input and quantum cost parameters and these parameters has defined in above.

Conventional One-Bit Comparator table comparison

one bit comparator design using existing gates with new BJN gate	Reversible gates	Garbage outputs	Constant inputs	Quantum Cost
Peres and BJN Gate	3	2	3	10
Toffoli and BJN Gate	4	2	3	16
Fredkin and BJN Gate	5	6	7	23
TR and BJN Gate	3	2	3	12

Proposed One-Bit Comparator table comparison

one bit comparator design using existing gates with new BVF gate	Reversible Gates	Garbage outputs	Constant inputs	Quantum cost
Peres and BVF Gate	3	2	2	8
Toffoli and BVF Gate	3	2	2	9
Fredkin and BVF Gate	3	3	2	9
TR and BVF Gate	3	1	2	7

Conventional One-Bit Comparator chart comparison

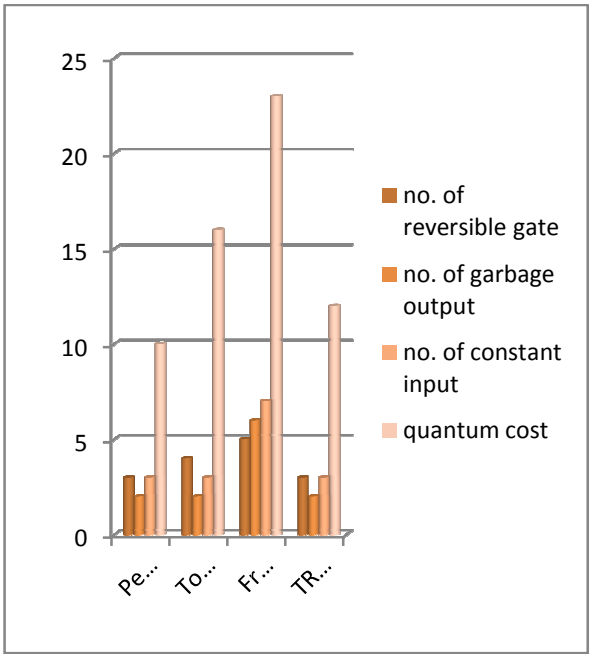


Chart 1.CONVENTOINAL Comparison Results

Proposed One-Bit Comparator chart comparison

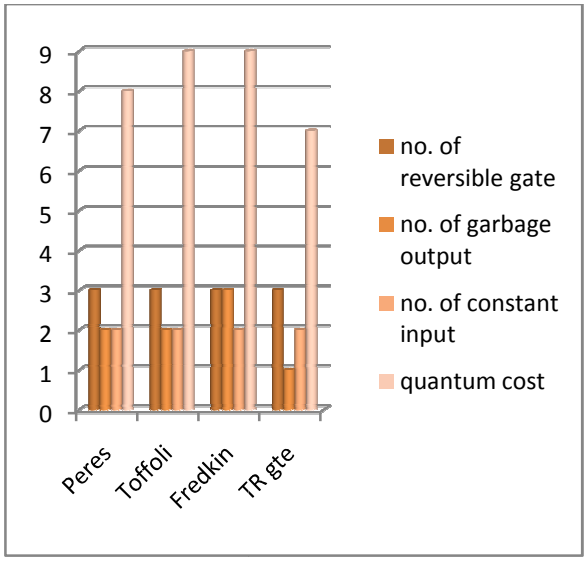


Chart 2 PROPOSED Comparison Results

CONCLUSIONS

The idea of this paper is an innovated reversible comparator which is implemented with the Reversible BVN gate. The design is very useful for the future computing techniques like ultra low power digital circuits and quantum computers.

In this paper we have tried to attain highly optimized One-bit comparator by using some of the basic reversible gates. The analysis of various implementations discussed are tabulated in Table and in chart.It gives the comparisons of the different designs in terms of the important design parameters like number of reversible gates, number of garbage outputs and number of constant inputs and quantum cost.

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