REAL TIME IMPLEMANTION OF STC AND FTC RADAR SYSTEM BASED ON FPGA

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Abstract

In this paper we are explosively the fundamental theory of radar system modules STC (sensitivity time control) or sea clutter and FTC (fast time constant) or rain clutter. The STC and FTC are commonly used to some clutter. The radar signal is widely used for weather forecast, air port traffic control, military and fire control. The system implements radar processing procedures in real time mode in FPGA (field programmable gate array). The FPGA device providing good performance of cheap platform for research and development. The compact structure of STC and FTC can Implementations of Xilinx FPGA using the generated VHDL code.

Index Terms**:** *FPGA, FTC, STC, LUT.*

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1. INTRODUCTION

Real time is correctness of system depend not only logical result of computation but also on which result are produced. Real time is over all correctness of the system depending upon both function correctness and timing correctness. Real time system command and process control system and multimedia and high speed communication system. Real time system is creating additional requirement. The radar is required to have a very good detection capability. Detection and track of small targets in harsh weather condition can help authorities in efficient monitoring of illegal activities. The radar device which is used to detection and ranging of contacts independent of time and weather condition, was one of the most important scientific discovery and technology. The radar signal processing is an excellent tool for weather prediction, civil aviation and many other applications including its military uses. The sensitivity time control and fast time constant are basic modules for radar signal processing that pretend to filter the echo's signal to decrease the effect of the mentioned clutters. The target recovering from the echo signal is not a trivial task since rain, snow, hail, or dust clutter affect radar's reading, resulting in poor or false target detection of the signal during time and space. In this paper we propose real time field programmable gate array implementations of STC and FTC radar modules.

2. MODULES

2.1 STC (Sensitivity Time Control)

Land -based radar have permanents echoes. Marine radar has sea clutter. Permanent echoes are the reflections form nearby objects: an air craft hanger, a building, a microwave tower, summit, etc. Except on the sophisticated commercial and military radar, there is nothing one can do with them except become familiar with these patterns. A high mounted antenna will shown "sea return" noise over a greater range, but the strength of this is quite weak. A low mounted antenna shows the interface over a smaller range; close in, but with strong echoes. The sea clutter control uses a special circuit to alter the receiver gain close to the ship, in such manner that the intensity of the clutter is reduced. This is makes it possible to work through the sea clutter ;however as the overall effect is to reduce the sensitivity of radar receiver close to the vessel ,weak returns from legitimate objects are likely to be weakened or completely suppressed. This control should be set to the least (brightest) total that can be tolerated. Always remember to zero the sea clutter control when the need for it has passed. Picking out small targets in sea clutter is what we want most from our radar. Large vessel sit well above the waves and have a good radar return in about all conditions. But smaller vessels are often lost in the radar clutter reflected back from waves. And, there is a tradeoff here between using tuning controls to reduce sea clutter and losing those small boat targets we really want to see. There are various controls on the 2117 which allow us to refine the image surrounding us in rough water. These include Rain and Sea Clutter, target averaging, and pulse length. In radar receivers, the wide distinction in return signal amplitudes make adjustment of the gain difficult. The adjustment of receiver gain for best visibility of nearby target return signals is not the best adjustment for distant target return signals. Circuits used to adjust amplifier gain with time, during a single pulse repetition period are called STC circuits, or "swept gain attenuator".

Local clutter levels dictate the magnitude of swept gain and conflicting requirements for swept gain are presented as the

antenna rotates. Modern systems dynamically measure clutter levels for a large numeral of cells within the coverage area of the radar. These measurements are slowly adjusted to take account of changing clutter levels and used to put the swept gain attenuator to an appropriate level for the range azimuth cell currently being processed. In most cases, the values used are a variation on the normal static law. This is due to abrupt changes in swept gain law destroying the integrity of the clutter amplitudes. in addition if long or compressed pulses are used, amplitude changes can affect the performance.

The STC is really a radar system term. Most modern radar system have a need to attenuate ,in a controlled Way, the amplitude of large target returns that may occur close to the trailing edge of the transmitted pulse. The moments of reading echo, it has high power due to the nearby and the last reading usually have a significant power decreasing. The responsible for correcting this sensitivity time control (STC) since it is commonly used to decrease the amplitude of nearby target that could be false target caused by sea clutter. In calm seas this control is set to its minimum value. STC's main task to detect close target that might be obscured by sea clutter, but if it is set to its high value trying to remove sea-clutter, STC could remove small close targets too. The figure 1 shows the kind of function used by the STC to correct sea clutter.

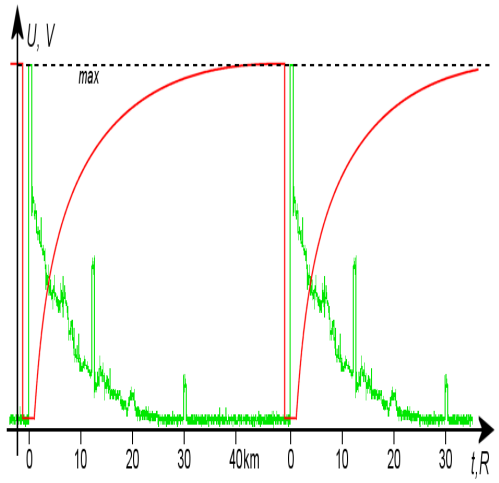

Figure 1. Echo and STC voltage Vs time (or distance).

This is accomplished through the use of a variable attenuator which is located someplace in receive channel behind the receiver protector. In a typical application, the attenuator is set to maximum attenuation during the period of the transmitter pulse. At the end of the pulse, the amount of attenuation is reduced, in a controlled way according to organization requirements, until it reaches 0 dB. In way, large close-in target returns are controlled and the effective dynamic range receiver is increased. The STC is really a programmed attenuation function.

2.2 FTC (Fast Time Constant)

The shorter wavelength radar is more susceptible to rain or snow meddling than are its longer wavelength cousins. A squall within your radar range can blanket the area of heavy rain with strong returns, twinkling somewhat like grass, but tending to obscure all other usable data in the vicinity. The rain clutter control will reduce the effect somewhat, allowing some ability to see targets within the area, However, like other clutter reducing circuit, this control also lower the overall sensitivity of the radar. Rain may be heavy on one azimuth arc only, and non-existent around the rest of the swept area. If the squall is not in an area of primary concern, level the clutter control at its minimum setting. Again, all anti-clutter control reduces the generally sensitivity of radar. Be in the habit of turning them off first, then adding back only the least sum needed to achieve a comfortable display viewing level. In addition to the rain control, some radar has a separate FTC control. This adjusts a circuits optimized for the diminution of precipitation interface at longer ranges. Rain , insects, and some weather condition like dust could be considered as noise for the radar signal , for these situations the Fast Time Constant(FTC) module is used to take away undesired reading , basically based on a derivative filter and now and then associated with CFAR (constant false alarm rate) used to set a constant probability of false echo. FTC sometimes called Rain clutter Control, Which is a variable FTC, is a differentiator that detects abrupt changes or fluctuations in echo's signal in order to discriminate constant or almost – constant echo's signal, frequently caused by rain, dust, snow or other unwanted echoes. It is also known as differential or anti-rain clutter control. FTC is in fact a high pass strain whose cost is reduction of maximum exposure range, to avoid this problem log –FTC could be used for large distances. When it is used to reduce the rain clutter is also called weather-fix. The rain clutter is a volumetric phenomenon so the amount of litter returned back to the radar will be directly proportional to the volume of the rain illuminated by the radar beam. Shown in figure2.

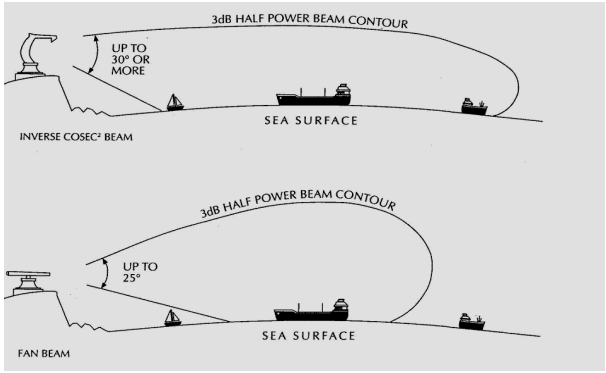

Figure 2 The shaped radar beam reduces rain clutter return and increases radar ranges.

3. ARCHITECTURE

The architecture of STC & FTC are require to the many elements like's control unit, mixer ,stream data and clock bus ,clock signal, output data bus look up table and ALU (arithmetic logic unit) etc. Each module the each module works independently from other two, then we propose a similar structural design based on stream data processing with one linear mixer that joins the two output. Show figure 3 is architecture proposed.

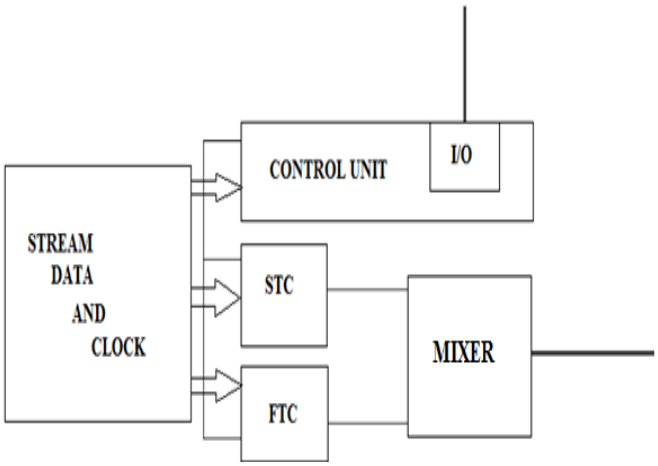

Figure 3. Architecture proposed.

The control unit work is initiate sequences of micro operation. Perform successively changing from one step to another step. The control unit receiver the control values for each two modules. The system arrangement the operation according to the range used and specifies input to each modules a fix occupation is used to process the STC those values are stored in the look up table. The LUT (look up table) is control the unit value is stored in look up table, but address addition to read this LUT could not be lineal due to different resolution and ranges used to radar's system. A stream data bus is data transfer between the personality control units. A clock signal regulates to flow of logic signal so that system can run optimum speed. A clock is devices that generate periodic signal for timing. Mixers are three port active or passive device are designed to yield both sum and difference frequency at a signal output port when two distinct input frequency are inserted into other two ports.

The STC module which elements are LUT (look up table), ALU (arithmetic logic unit), a counter and a register to store output data. LUT is used as STC's curve storage, the counter is calculated to configure its increment as function of resolution and counter's function is provide the LUT's address. Shows figure 4.

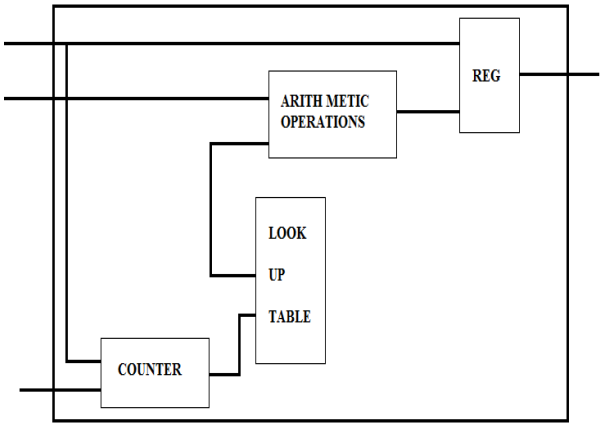

Figure 4 sensitivity time control architecture.

FTC is basically a driver which is built with an adder and two register, one to store the previous value and other to store output. The register store temporary result related to the computation. There are also special purpose register used to by the control unit. Shown in figure 5.

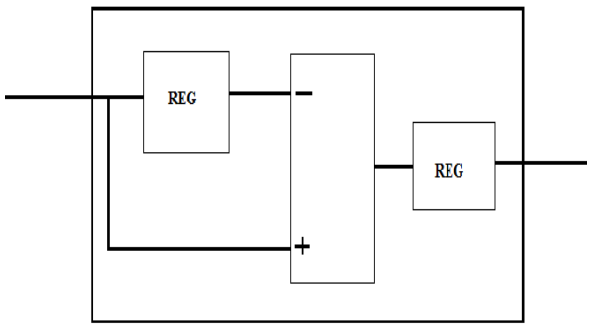

Figure 5.fast time constant architecture.

4. HARDWARE IMPLIMENTATION

The main objective in this section is to demonstrate a functioning hard ware for the purposed STC & FTC architecture. The mat lab is high performance language for technical computing mat lab is modern programming language. The hardware realization, a simulation using mat lab was performed using a synthetic echo is 12 bit integers and 2048 samples. The result of simulating was to validate the results obtained by hardware once it is implemented and also to use the same synthetic echo to test the implementation. The output of the copying of a synthetic echo through the two mixed modules, the signal with highest and lowest values is the synthetic echo and the order is the filtered echo (darker and marked one).shown in figure 6.

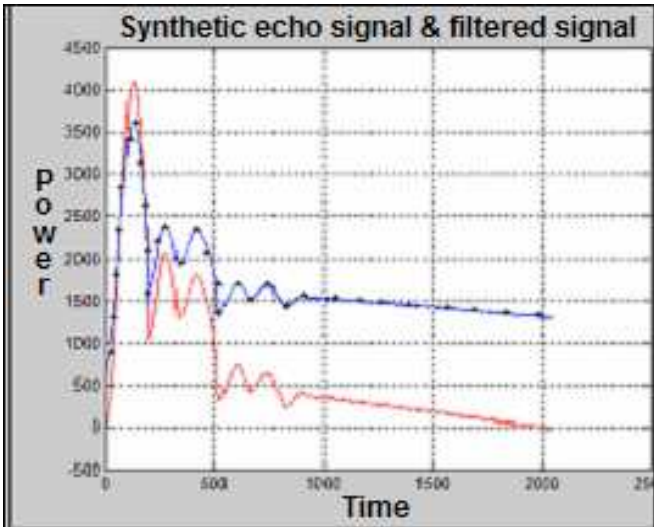

Figure 6. Hardware implementation performed with Mat Lab

5. FPGA IMPLEMENTATION

The implementation was performed in a Xilinx Spartan II FPGA. The FPGA is large array of configuration of logic block connected via programmable inter connects. The modern FPGA have very resourceful I/O blocks which make them easy to interface to other chip. The system was developed with VHDL Hardware Description Language coding simulating tool. The VHDL provides a rich of concurrent statement to module the concurrency in digital hardware. The VHDL is strongly type talking in the first stages of design and to generate some of the basic elements; at figure 7 it is shown the block design at on the go HDL.

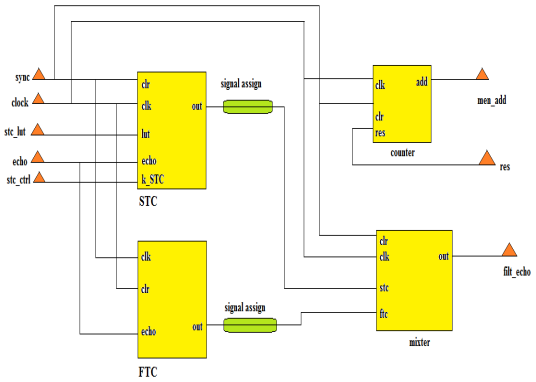

Figure 7 Block design in Active-HDL.

The main advantage of proposed structure (the software and FPGA hard ware) is the facility whereupon we can easily change the parameters of each block of the system. it is required in some application to increase the precision of the system, let us elasticity to adjust the parameter of the system ,and therefore better solutions. VHDL model was synthesize with Xilinx ISE and targeted for a XC2S50TQ144-5(Spartan II). ISE core generator was used for the STC LUT creation. Finally Mat Lab was used for simulation, generating STC values and its S-Record and plotting the results stored at the board SDRAM. In order to confirm the hard ware accomplishment a test bench was implemented. It is basically a SDRAM driver to read the synthetic echo, stored via S-record, and also used storing output stream. The drinkable signal, resulted of the hardware implementation is like the one replicated with Mat Lab. Some minor difference result from the limited memory for the LUT that stores STC values allocated at the BRAMs of the FPGA. The system realization throughput is one sample per clock cycle. According with minimum period of 9.787 ns, the maximum frequency is 102.176 MHz.

6. RESULTS

The implementation of STC & FTC on radar system based on FPGA in real time mode. The trial result measured in the implemented radar processing model presented the copied echo signal & filtered signal by the proposed architecture is shown in figure 7.

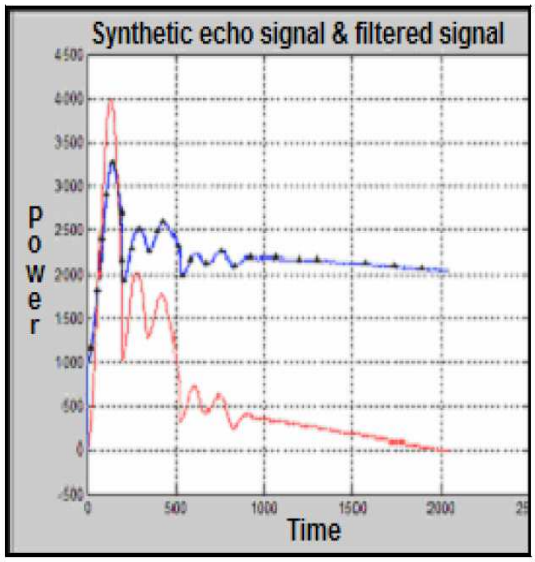

Figure 8 Result obtained.

7. DISCUSSION

The proposed parallel architecture implements STC and FTC modules with some and specialized dedicated hard ware. This implementation perform the arithmetic operations needed to process STC and FTC concurrently, has latency of one cycle and produces an output result on each clock cycle. The planned architecture process data on stream basis and the number of samples does not modify the latency. since its maximum frequency is around 100 MHz and sample is

processed by cycle, processing 100MSPS (Millions of samples per second) could be reached, and it is as good as profitable radar that process between 50 and 100 MSPS. marketable radar process 4096*4096 sample in 2.5 second which means 6710886.4 samples per second .

CONCLUSIONS

This work presents an efficient implementation of STC and FTC in real time. The designed architecture for those controls is based on similar dealing out under dedicated and specialized hardware that was reached due to bendable and chip platform provided by FPGA. Therefore this programmable hardware with its significant improvement in the processing speed will make it possible to augment the decision of the radar range cell and open new avenues for further useful real time application. The presented building is able to process 100 MSPS (millions of sample per second).Which is a good metric according with commercial radars.

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