HIGH PERFORMANCE NOVEL DUAL STACK GATING TECHNIQUE FOR REDUCTION OF GROUND BOUNCE

K. Srinivasa Rao [1] Ravinder Kaur [2], Palwinder Kaur [3]

[1] *HOD, Electronics & Communication Engineering, TRR Engineering College, A.P, India,* ***jntuksr@gmail.com***
[2] *Assistant Professor, Electronics & Comm. Engineering, TRR Engineering College, A.P, India ,****ravinder.atpl@gmail.com***
[3]*Student, Electronics & Comm. Engg. Chandigarh Engineering College, Punjab, India,* ***palwinder.08066@gmail.com***

Abstract

The development of digital integrated circuits is challenged by higher power consumption. The combination of higher clock speeds, greater functional integration, and smaller process geometries has contributed to significant growth in power density. Today leakage power has become an increasingly important issue in processor hardware and software design. So to reduce the leakages in the circuit many low power strategies are identified and experiments are carried out. But the leakage due to ground connection to the active part of the circuit is very higher than all other leakages. As it is mainly due to the back EMF of the ground connection we are calling it as ground bounce noise. To reduce this noise, different methodologies are designed. In this paper, a number of critical considerations in the sleep transistor design and implementation includes header or footer switch selection, sleep transistor distribution choices and sleep transistor gate length, width and body bias optimization for area, leakage and efficiency. Novel dual stack technique is proposed that reduces not only the leakage power but also dynamic power. The previous techniques are summarized and compared with this new approach and comparison of both the techniques is done with the help of Digital Schematic(DSCH) and Microwind low power tools. Stacking power gating technique has been analyzed and the conditions for the important design parameters (Minimum ground bounce noise) have been derived. The Monte-Carlo simulation is performed in Microwind to calculate the values of all the needed parameters for comparison.

Index Terms: *Ground Bounce Noise ,Power gating schemes ,Static power dissipation, Dynamic power dissipation, Power gating parameters, Sleep transistors, Novel dual stack approach, Transistor leakage power*

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1. INTRODUCTION

Ground bounce noise comes into effect when the ground connection becomes unable to handle the excess voltage. As a result a back e.m.f is produced that bounces back towards the transistor and makes the transistor on. The ground bounce puts the input of a flip flop effectively at a voltage level that is neither a one nor a zero at clock time. The ground bounce also affects the clock signal. A similar phenomenon may be seen on the collector side, called V_{CC} sag, where the bounce noise makes the V_{CC} value unnaturally low.

2. FACTORS AFFECTING GROUND BOUNCE

2.1 Load

The load affects ground bounce directly. The larger the capacitance of the test system, the larger ground bounce will be. There is little the designer or test developer can do to change this, since the test platform is usually beyond their control. Lumped loads, such as those at the test system, have a larger affect on the ground bounce level than an equivalent distributed load.

2.2 Speed

Higher speeds make ground bounce worse. Here the concern is not MHz, but the output characteristics of the devices under test. Outputs that switch rapidly (large dV/dt) and can provide large output currents (large dI/dt) will cause greater ground bounce. Board designers can reduce test related ground bounce problems by using the slowest logic family (dV/dt) that will allow them to achieve their required system speed (MHz).

2.3 Drive Currents

Another area where designers can help, especially when using programmable logic devices, is to choose output cells with lower drive currents. When the large number of outputs will switch simultaneously, the large transient current will generate the bounce noise. So we can select those test patterns where the number of pins switching at a time is limited. Large boundary scan tests are particularly susceptible to ground bounce problems, because the test patterns involve large numbers of pins changing state simultaneously.

3. POWER GATING TECHNIQUE

Power gating technique is used to reduce the leakage power .It uses high threshold voltage sleep transistors which cut off VDD from a circuit block when the block is not switching..Power gating uses low-leakage PMOS transistors as header switches to shut off power supplies to parts of a design in standby or sleep mode. NMOS footer switches can also be used as sleep transistors.

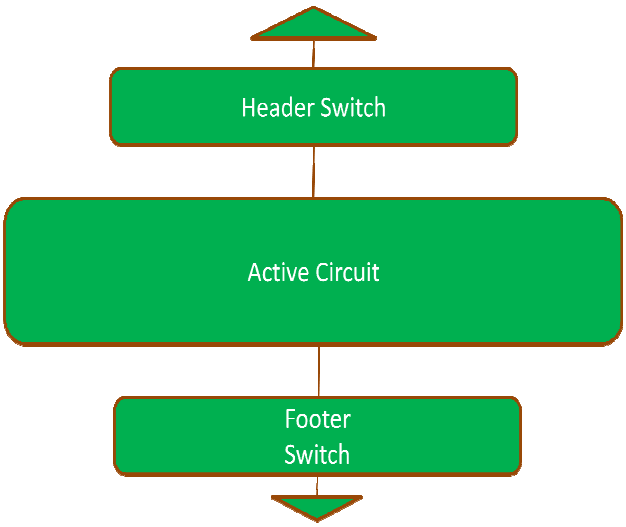

Fig-1: Power gating enhancement process

4. DUAL STACK APPROACH

The dual stack approach consists of a chain of 4 inverters. In this section, the structure and operation of novel low-leakage-power design is described. It is also compared with well-known previous approaches, i.e., the sleepy stack, dual sleep and sleep transistor methods. First we explain the circuit operation for a chain of 4 inverters in sleep mode.

In sleep mode, the sleep transistors are off, i.e. transistor N5 and P5 are off. We do so by making S=0 and hence S'=1. Now we see that the other 4 transistors P6, P7 and N6, N7 connect the main circuit with power rail. Here we use 2 PMOS in the pull-down network and 2 nmos in the pull-up Network. The advantage is that NMOS degrades the high logic level while PMOS degrades the low logic level. Due to the body effect, they further decrease the voltage level.

So, the pass transistors decreases the voltage applied across the main circuit. As we know that static power is proportional to the voltage applied, with the reduced voltage the power decreases but we get the advantage of state retention. Another advantage is got during off mode if we increase the threshold voltage of N6, N7 and P6, P7.

The transistors are held in reverse body bias. As a result their threshold is high. High threshold voltage causes low leakage current and hence low leakage power. If we use minimum size transistors, i.e. aspect ratio of 1, we again get low leakage power due to low leakage current.

As a result of stacking, P6 and N6 have less drain voltage. So, the DIBL effect is less for them and they cause high barrier for leakage current. While in active mode i.e. S=1 and S'=0, both the sleep transistors (N5 and P5) and the parallel transistors (N6, N7 and P6, P7) are on. They work as transmission gate and the power connection is again established in uncorrupted way. Further they decrease the dynamic power.

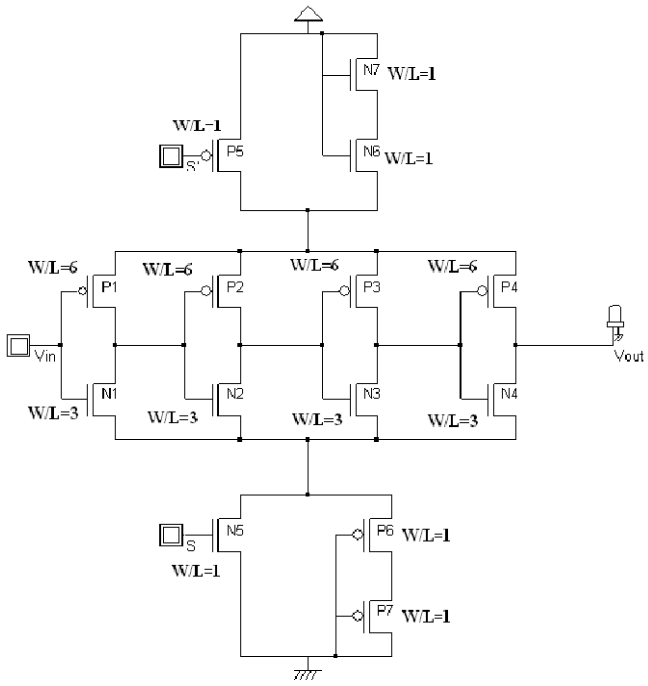

Fig - 2: Dual stack approach

Power gating circuits most probably reduce the complexity of the circuit, which leads to power consumption reduction.

5. SIMULATION ENVIRONMENT

The simulation parameters have been analyzed with the help of the Microwind tool (version 2) and DSCH (version 2) for the schematic verification.

5.1 DSCH (Digital Schematic)

The DSCH program is a logic editor and simulator. DSCH is used to validate the architecture of the logic circuit before the microelectronics design is started. DSCH provides a user-friendly environment for hierarchical logic design, and fast simulation with delay analysis, which allows the design and validation of complex logic structures.

DSCH also features the symbols, models and assembly support for 8051 and 16F84 controllers. The highlights are:-

- Supports Hierarchical logic design.
- Generates a Verilog description of the schematic for layout conversion.
- Immediate access to symbol properties (Delay & Fan-out)
- Model and assembly support for 8051 and PIC 16F84 Microcontrollers.
- Sub-Micron, Deep – submicron and nanoscale technology support.

5.2 Microwind

The Microwind is a tool for designing and simulating circuits at layout level. The tool features full editing facilities (copy, cut, past, duplicate, move), various views (MOS characteristics, 2D cross section, 3D process viewer), and an analog simulator. The Microwind program allows designing and simulating an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. The Microwind includes all the commands for a mask editor as well as original tools never gathered before in a single module (2D and 3D process view, Verilog compiler, tutorial on MOS devices). You can gain access to Circuit Simulation by pressing one single key. The electric extraction of your circuit is automatically performed and the analog simulator produces voltage and current curves immediately.

6. METHODOLOGIES

The Methodology consists of 3 Modules.

- Logic circuit design, simulation, and Verilog file generation using DSCH.
- Layout design using MICROWIND.
- Simulation.

Here the Conventional technique corresponds to simple chain of 4 invertors without using Power gating approach. In the analysis this circuit is mentioned as Base Circuit.
And the Modified technique corresponds to chain of 4 invertors using Power Gating Approach and mentioned as Design 1 in the analysis. The proposed design i.e Novel dual stack approach uses 0.12µm technology and operated with 1.2V supply voltage.

7. MODULE 1

7.1 Designing logic circuit using DSCH

7.1.1 Design 1

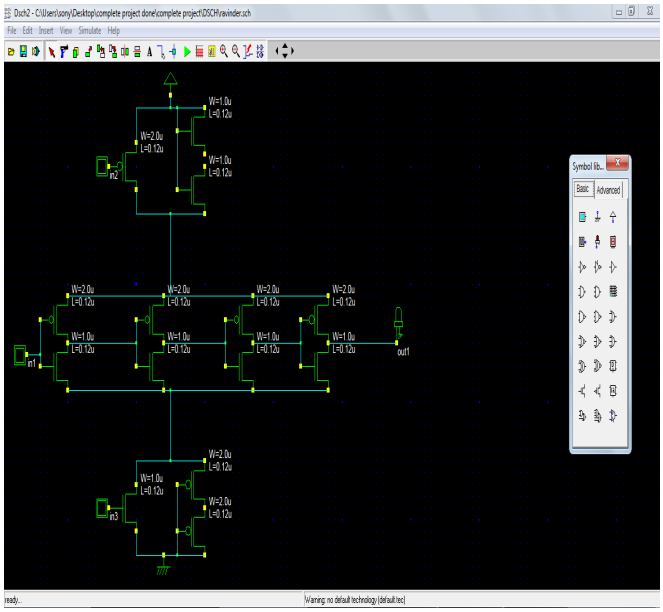

Fig-3: Design 1 in DSCH

7.1.2 Base Design

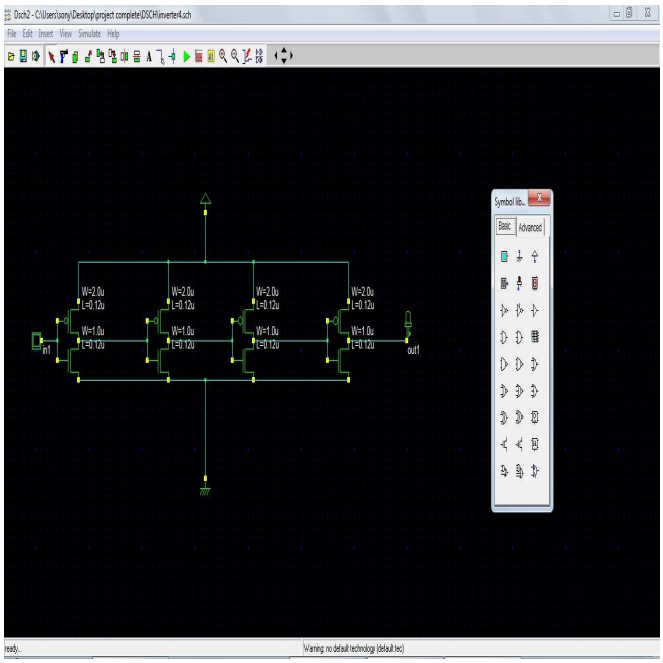

Fig-4: Base design in DSCH

7.2 Circuit Simulation

The pin states and the wire states are indicated after simulation of the circuit. We can provide different inputs and we can check the corresponding output. Simulation also indicates the active and non-active parts of the circuit.

7.2.1 Design 1

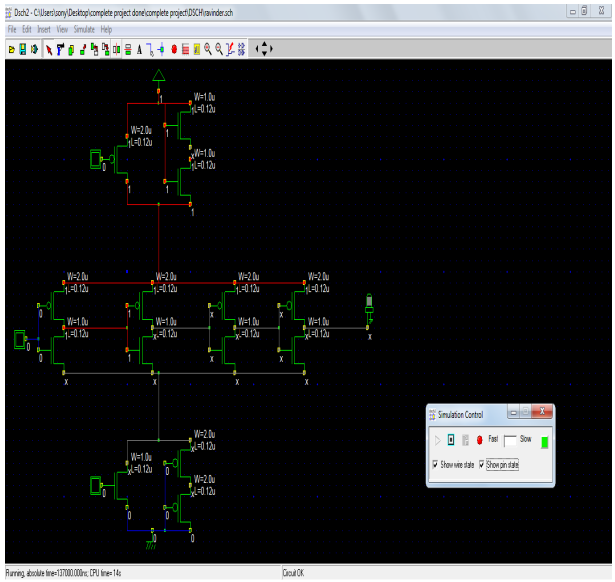

Fig-5: Design 1 circuit simulation

7.2.2 Base Design

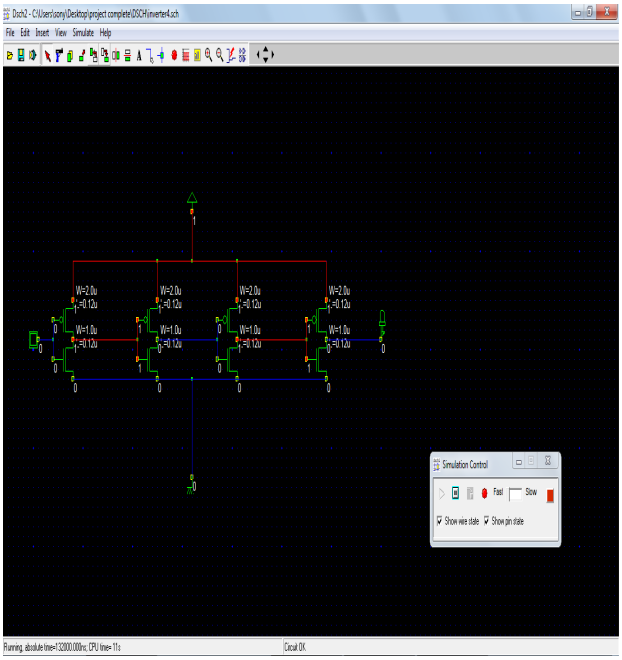

Fig-6: Base design circuit simulation

7.3 Generating Verilog File

When the circuit is simulated in DSCH , the Verilog file is generated. This file is saved as .txt extension. This Verilog file is compiled in Microwind to design the layout of the circuit.

7.3.1 Design 1

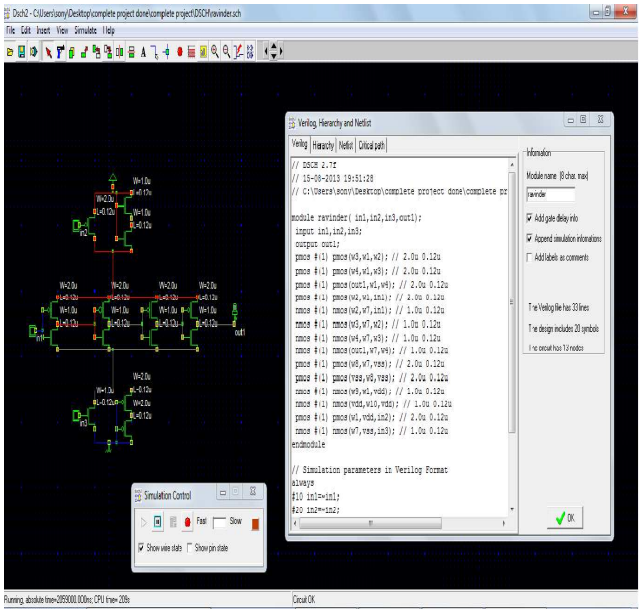

Fig-7: Design 1 verilog file

7.3.2 Base Design

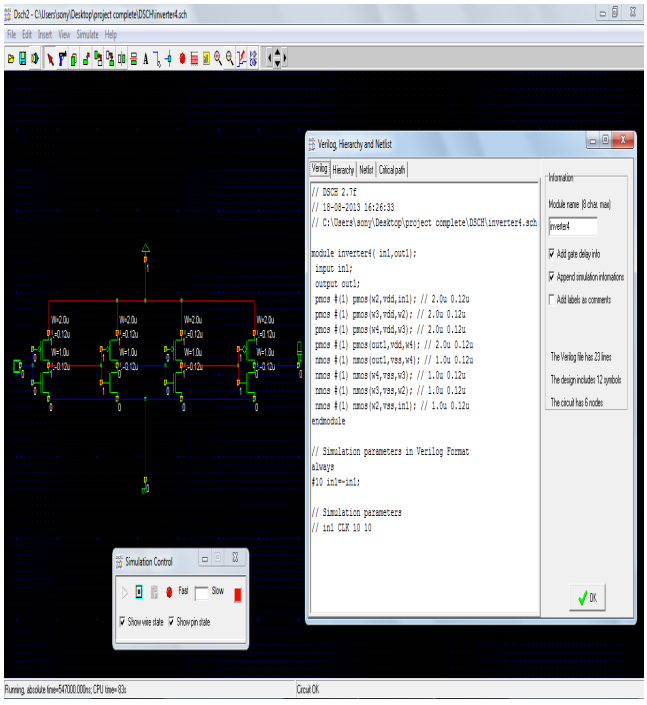

Fig-8: Base design Verilog file

8. MODULE 2

8.1 Design 1

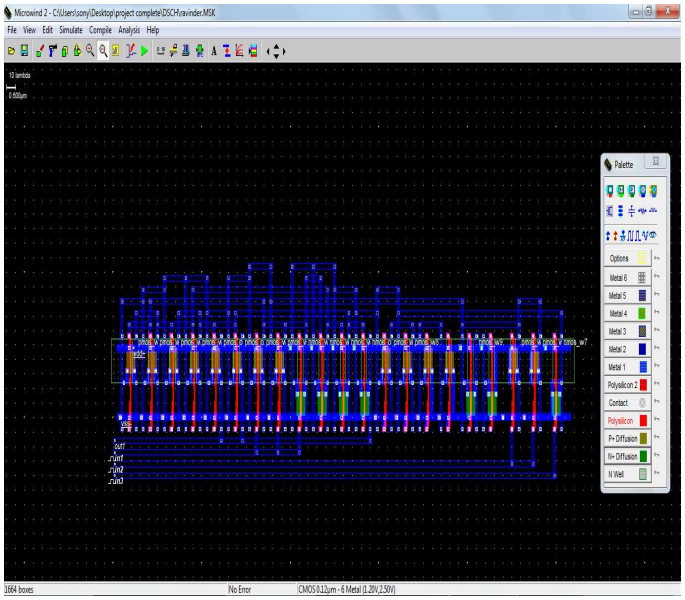

Fig-9: Design 1 layout

8.2 Base Design

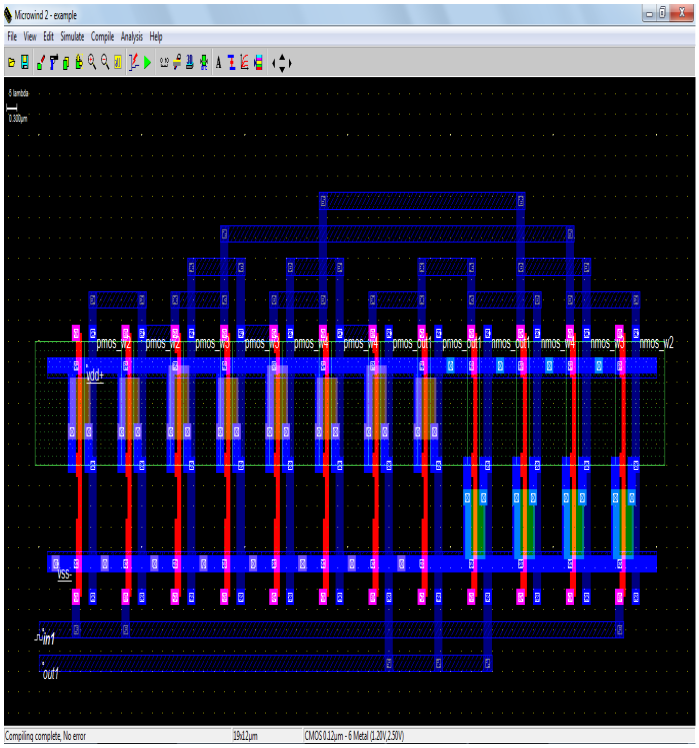

Fig-10: Base design layout

9. MODULE 3

9.1 Design 1 Voltage versus Time

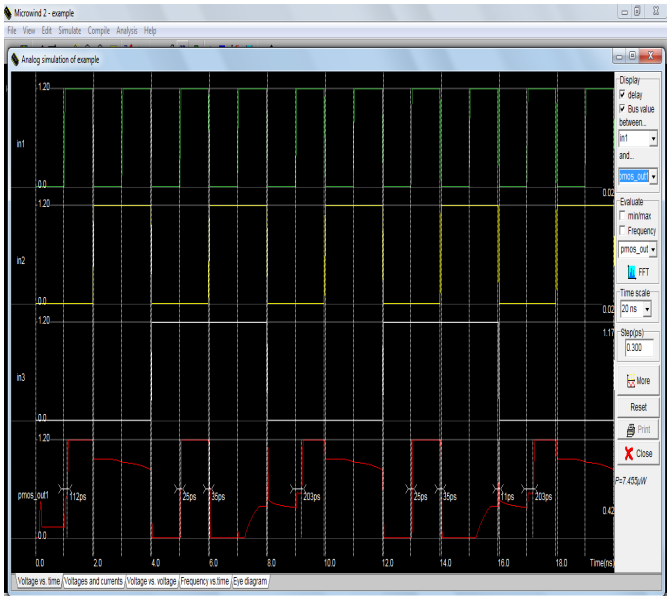

Fig-11: Design 1 voltage versus time waveform

9.2 Base Design Voltage versus Time

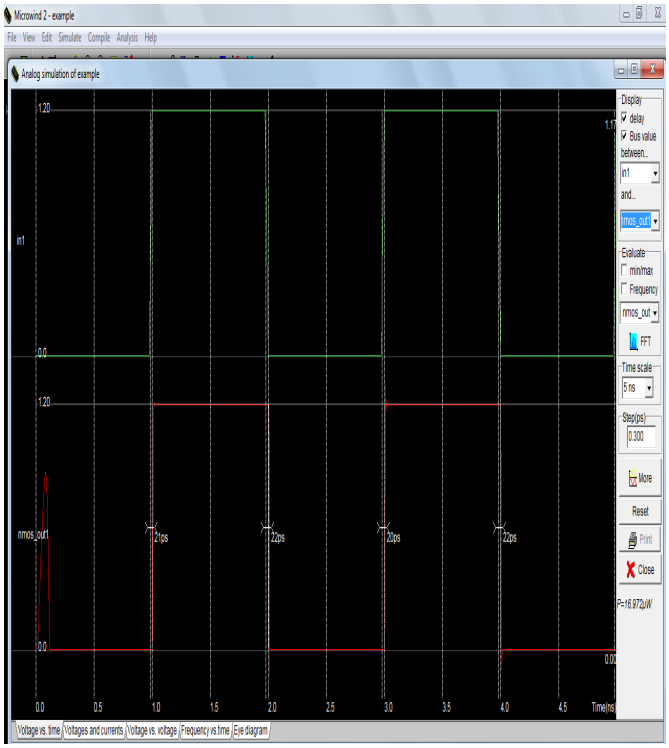

Fig-12: Base design voltage versus time waveform

9.3 Design 1 Voltages and Currents versus Time

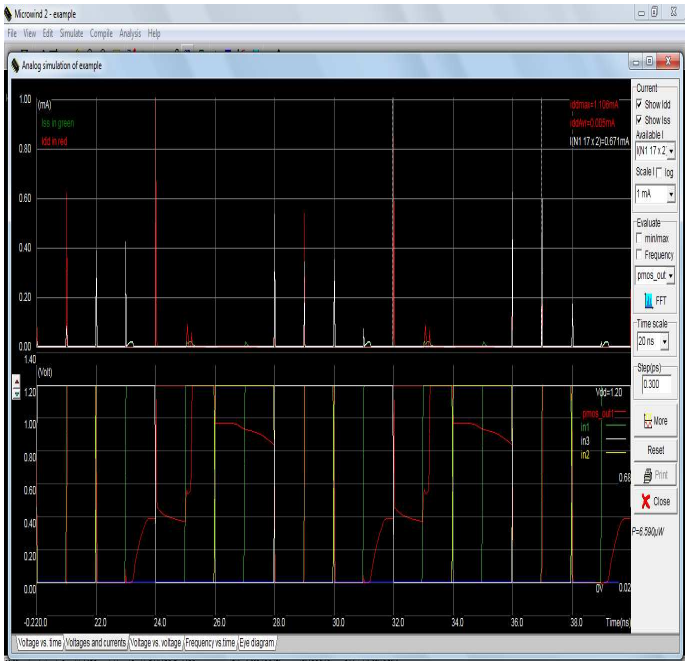

Fig-13: Design1voltages and currents versus time waveform

9.4 Base Design Voltages and Currents versus Time

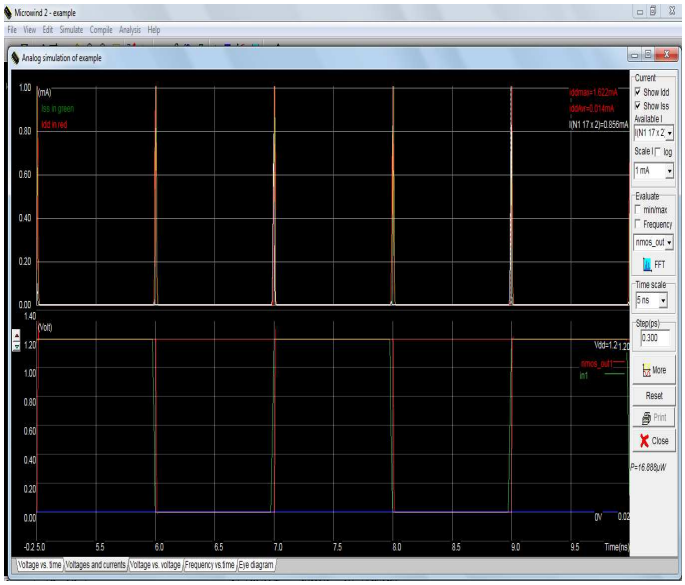

Fig-14: Base Design voltages and currents versus time waveform

10. RESULTS

The results are based on the comparison between the Design 1 and Base design parameters. To get the parameters for comparison Monte-Carle Simulation is done.

Table- 1: Parameters of Design 1

DESIGN 1				
SR. NO.	FREQ (GHZ)	FINAL VOLTAGE (V)	MAX Idd (mA)	POWER DISSIPATION (µW)
1	0.91	0.021	1.26	8
2	0.885	0.078	1.164	7
3	0.915	1.03	1.205	7
4	0.85	0.021	1.027	7
5	0.91	0.015	1.224	8
6	0.899	1.04	1.09	7
7	0.827	0.021	1.075	8
8	0.8	0.099	1.01	7
9	0.932	1.038	1.131	8
10	0.85	0.039	1.195	8

Table- 2: Parameters of Base Design

BASE DESIGN				
SR. NO.	FREQ (GHZ)	FINAL VOLTAGE (V)	MAX Idd (mA)	POWER DISSIPATION (µW)
1	0.5	0	1.621	17
2	0.5	0	1.217	18
3	0.5	0	1.36	17
4	0.5	0	2.151	16
5	0.5	0	1.657	17
6	0.5	0	1.657	19
7	0.5	0	1.509	16
8	0.5	0	1.947	19
9	0.5	0	1.731	17
10	0.5	0	1.471	18

CONCLUSIONS

Using the proposed Novel technique the ground bounce noise is reduced to about 2.56 times compared to without applying the technique. Noise immunity has been carefully considered since significant threshold current of the low threshold voltage transition becomes more susceptible to noise. The above analysis shows that the power dissipation in Base circuit is 17.4 µW (average value) and 7.5 µW (average value) in Design 1. Clearly the Proposed Power gating technique is saving 57 % of the power.

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BIOGRAPHIES

K. Srinivasa Rao, HOD, Electronics & Comm. Engineering, TRR Engineering College, Andhra Pradesh, India

Ms. Ravinder Kaur , Assistant Professor, Electronics & Comm. Engineering, TRR Engineering College, Andhra Pradesh, India

Ms. Palwinder Kaur, Student Electronics & Comm. Engineering, Chandigarh Engineering College, Punjab, India