COUNTER-BASED DESIGN OF DPLL FOR WIRELESS COMMUNICATION

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Abstract

For proper reception of the transmitted data, the design of effective demodulation schemes plays a very crucial role. In the earlier times, some of the traditional techniques like envelope detection etc were utilized for demodulation purposes. However, these techniques, although could be implemented without much difficulty, but at times, when the extent of interference due to the surroundings, system noise and other degrading parameters were very significant, these traditional techniques were found to be non-sensitive to these large-scale effects. To overcome these shortcomings, over the years, the device called phase locked loop has gained much popularity. This device, having the capacity to recover the phase of the transmitted pulse, is capable of yielding very accurate approximations of the transmitted pulses and thus accounts for very low values of bit error rates. Considering the utility of the device, in the recent times, it has been attempted to provide a sound digital design for the device so that the design complexity of the device could be overcome by replacing its integral parts with simplified digital circuits and also would improve the noise performance of the device. With this view in mind, in this piece, we put forward a design of the Digital Phase Locked Loop (DPLL) using a counter based logic. Here, the essential components of the DPLL have been implemented using logic circuits and counters and further, while doing so, the requirement of the components of a traditional PLL has also been minimized.

Index Terms: *Counter oscillator, detector, phase, recovery etc*

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1. INTRODUCTION

A phase locked loop is a control system that tries to generate an output signal whose phase is related to the phase of the input reference signal [1]. It consists of a phase detector, loop filter and voltage control oscillator as feedback. This circuit compares the phase of the input signal with the phase of the signal derived from its output oscillator and adjusts the frequency of its oscillator to keep the phases matched. The signal from the phase detector is used to control the oscillator in a feedback loop. Consequently the phase detector loop can track an input frequency or it can generate a frequency multiple of the input frequency. The former property is called demodulation and the latter property is used for indirect frequency synthesis [2]. The digital version of PLL is Digital PLL. Basically DPLL consists of a digital phase detector realized using XOR gates, J.K, flip-flops etc. It also consists of digital loop filter which is designed using the fundamental design procedures for digital filters in signal processing. Also it consists of a feedback element which is a discrete time version of voltage controlled oscillator (VCO) is also sometimes known as digitally controlled oscillator (DCO) or numerically controlled oscillator (NCO). This feedback element generates the input reference signal and the phase detector detects the difference in phase of the incoming signal and the reference signal. The loop filter is used for removing the high frequency randomness. The DPLL thus corrects and locks the phase of incoming signal and the reference signal and due to it the frequencies. are also locked giving at the output a replica of the original message pulse but with much improved noise performance and less design complexity. The later version of DPLL is the All Digital Phase Locked Loop (ADPLL). ADPLL is an implementation of PLL with all digital components. The ADPLL is now most widely used since FPGA is an exclusively a digital device in which the ADPLL is to be implemented.

2. THEORETICAL BACKGROUND

The All Digital Phase Locked Loop is a digital PLL which is implemented only by digital blocks. ADPLL consists of the same parts that is present in PLL i.e. phase detector, loop filter and voltage controlled oscillator which are implemented in purely digital circuits. The input to the ADPLL is a digital stream normally from an analog to digital converter or a clock. The approach for the design of DPLL is counter based approach. The block diagram of counter based DPLL is shown in figure1.

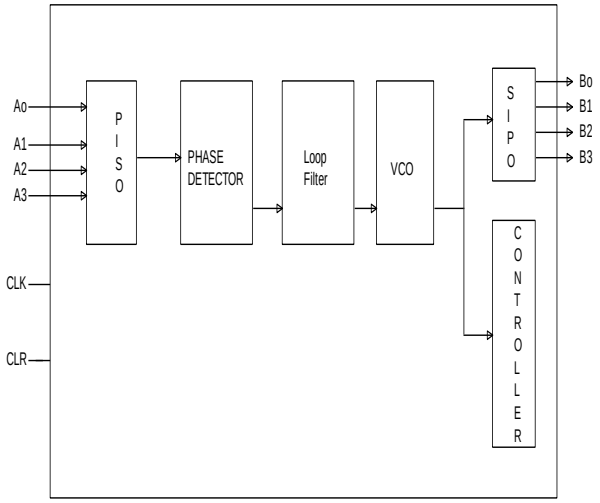

Figure1: Block Diagram of Counter Based DPLL

2.1 Explanation of the Block Diagram

The first block of counter based DPLL is the parallel in serial out (PISO) whose task is to give output one by one with respect to the clock. The second block is the phase detector which is designed using XOR based logic to detect the phase in between the input and reference signal [3]. The 3rd block is the counter based loop filter. The task of this block is to count for how many times the input bit differs from the reference bit. The fourth block is the counter based VCO whose task is to generate the same bit as that of the input bit. The fifth block is the controller, which locks the whole system once the message signal is out. The sixth block is the Serial in parallel out (SIPO). From SIPO, we will get the recovered clock signal i.e. the originally used carrier frequency at the transmitter end.

2.2 DPLL Based Wireless Communication Link

In the above discussion, we have mainly focused on the behavior and design aspects of the DPLL as a stand-alone device. However, the actual significance of the device can be realized only when its performance is analyzed when in use in a practical real-time setup. In this regard, the device that has been proposed for use in a practical wireless communication system. The DPLL is very useful when used in the receiver part of the link. It provides very accurate results when used fr demodulation purposes largely due to the fact that it has a very unique principle of operation which aims at capturing the phase of the originally transmitted signal and thus recovers the signal properly from the effects of degradation of the wireless environment. It also saves the extra overhead of equalizer design as in traditional systems. However, a very important aspect that should be noted here is that there should a proper linking interface between the proposed DPLL device and the wireless link i.e. the channel. This is because the system that we have proposed is an exclusively digital setup whereas the received signal from the wireless channel has a purely analog domain behavior. So, for proper functioning of the DPLL in the wireless setup, it becomes very crucial to have a proper interface between the wireless link and the DPLL receiver which provides for a translation from analog domain to digital domain behavior and vice-versa at the output of the receiver.

3. LITERATURE SURVEY

Based on DPLL, various researches are going on and in this section some of the related works carried out in the recent years are discussed. The design and modeling of ADPLL in purely behavioral mode in which the modeling of digital phase detector and also the explanation of the stability issues related with asynchronous operation of digital PFD is carried out [4]. The ADPLL can also be designed in 0.25 micron CMOS technology and the locking of phase is achieved in about 100 reference clock cycles and it is found that the performance of digital PLL is better than that of analog PLL because of its less sensitive to noise and operating conditions [5]. Also ADPLL can be designed based on popular sequential circuits and it is implemented in FPGA [6]. In the design and implementation of different multipliers using VHDL, a comparison is made for different multipliers with respect to the design complexities, speed of operation etc. to find the optimum design from a number of sequential and combinational designs [7]. Moreover in the design of DPLL the most valued aspect of the work is that after developing the components of the DPLL it was tested for QPSK modulated signal and it was found that it has better BER performance than the existing PLL technology thus giving a breakthrough in this field [8].

4. WORKING MODEL

In counter-based logic design we are using counter-based logic for designing the loop filter and the VCO. In digital domain the task of loop filter is to count for many times the bits are consecutively mismatched. we have found that the task of loop filter and VCO is same, so we can neglect the loop filter, as we are trying to recover the clock signal which we are getting from the VCO without using the loop filter. The circuit level diagram of counter based DPLL is shown in the Figure 2.

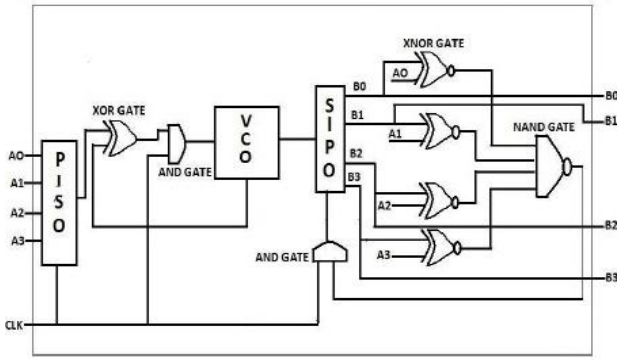

Figure 2: Counter Based DPLL

- The first block is parallel in serial out(PISO). It is used so that the message signals do not come in burst to the receiver. It is designed such a way that for a input data bit stream say for 4bit, at one clock the first bit is faded to the DPLL. At the second clock, the next bit and so on.
- The next is the phase detector which is designed using simple XOR gate. When there is mismatch between the incoming bit and the reference bit from VCO, it will give high output i.e. '1', or else it will give 0.
- Next is the VCO. To control the operation of the VCO, we are using an AND gate, whose input is the output of the XOR gate and the master clock. So when the output of the XOR gate is '1', AND gate will give output as '1', which is faded as the clock for the VCO. VCO is designed using counter based logic. The task of this logic is to generate the same bit as that of the input bit.
- The next block is serial in parallel out (SIPO). It is used so that we get the output parallelely.
- The next small circuit comprises the Controller block. It is designed using the basic combinational gates. It is used to lock the whole system. After getting the output we are checking each output bit to the input bit using the XNOR logic. When it is matched it will give '1', or else it will give '0'. So when all the bits are matched so all the outputs will be '1', giving the NAND gate output as '0'. Then we are using AND gate whose output is faded as clock to the SIPO. So when all the bits are matched, the AND gate will give '0' output, so SIPO will not operate, thus the system will be locked, and we are able to recover the clock signal.

5. RESULTS and DISCUSSION

The schematic diagram of counter-based DPLL is shown in figure 3.

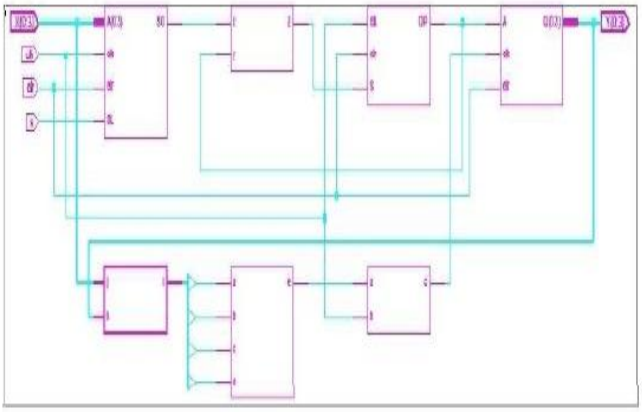

Figure 3: Schematic diagram of counter-based DPLL

In the Figure 3, as can be seen above, the RTL schematic is depicted that has been generated from the hardware simulation tool. It shows the basic building blocks that are involved in the design of the proposed device. The schematic diagram depicts that the system takes input as a four bit data and subsequently there co-exist a number of combinational as well as sequential blocks. Some of these blocks such as the counter etc which are sequential in nature are used for generation of the oscillation and for the purpose of matching the locally generated pulse with the incoming reference pulse whereas the combinational blocks are used for controller action and locking the device at the accurate state.

The output waveform of counter-based DPLL is shown in figure 4.

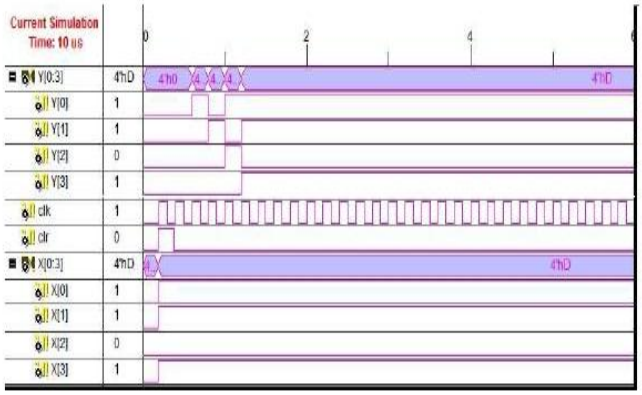

Figure 4: Output Waveform of Counter-Based DPLL

From figure 4, it is seen that four bit data is given as input signal to the PISO and after one clock a single bit is fed to the phase detector. Then the bit is compared with VCO's output and at the 4th clock we are able to recover the clock, and it will be locked for the rest of the clock. We get the final four bit data from the SIPO.

6. ADVANTAGES AND LIMITATIONS

6.1 Advantages of Counter-Based Design of DPLL

- The counter based DPLL that we have proposed uses common circuitry for each bit of the data to be processed and as a result the computational and design complexity is less and also the hardware requirement is minimized. This is largely attributed to the fact that the design is such that at each instant, one bit of data is recovered which is controlled by a Serial-In-Parallel-Out Buffer at the input of the DPLL.
- Traditional communication systems needed an equalizer unit at the receiver section because the demodulators in the past were not sufficiently strong

to retrieve the message pulse. But, the DPLL is a very powerful demodulation device and due to its unique characteristic of recovering the phase of the signals, it can independently work as the receiver without the use of an equalizer thus reducing the additional designing and cost overheads.

6.2 Limitations of Counter-Based Design of DPLL

Although the design for the DPLL proposed by us has its plus points over the traditional designs that have been suggested over these years, specifically with regards to the requirement of minimum hardware, but it also has its own set of limitations. The DPLL we have proposed for takes more than a single clock to lock the locally generated signal with respect to the reference signal. In fact, it has been experimentally found that the number of clocks required to lock a particular data is same as the number of bits that are used to represent the data. Thus, the speed of the device proposed would be very less when we implement it for a system which uses large number of bits for data representation. Also, as it takes more than a clock, to perform the operation, so after the first set of data is sent ,the second set of data can be sent only when the first data set is locked and thus if proper control is not maintained, it might lead to de-synchronization or mismatch.

CONCLUSIONS

Based on our above discussion, we can state that the DPLL is undoubtedly a very useful and versatile device. It can find huge applications in not only communication setups but also in other stand alone applications like clock recovery circuits of computers, frequency processing devices like frequency multiplier, divider etc. The design for the DPLL that has been proposed here can be used in a large pool of activities starting from designing of an independent DPLL based communication system to recovering the system clock in PCs etc. Distinct preferences to the design for use in real time and industrial applications is attributed mainly to the fact that the design procedure is very simplified and built up around the basic building blocks of digital circuitry and in addition to it the designing cost is a major advantage. However, care should be taken in real time applications related to the synchronization of the other elements of the setup to the proposed device. A separate synchronization unit is suggested to be used for the device so that there is no mismatch.

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