A CONTINUOUS-TIME ADC AND DIGITAL SIGNAL PROCESSING SYSTEM FOR SMART DUST AND WIRELESS SENSOR APPLICATIONS

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Abstract

In this paper an event-driven (ED) digital signal processing system (DSP), Analog-to-digital converter (ADC) and Digital-to-analog converter (DAC) operating in continuous-time (CT) with smart dust as the target application is presented. The benefits of the CT system compared to its conventional counterpart are lower in-band quantization noise and no requirement of a clock generator and anti-aliasing filter, which makes it suitable for processing burst-type data signals.

A clock less EDADC system based on a CT delta modulation (DM) technique is used. The ADC output is digital data, continuous in time, known as "data token". The ADC used an un buffered, area efficient, segmented resistor string (R-string) feedback DAC. This DAC in component reduction with prior art shown nearly 87.5% reduction of resistors and switches in the DAC and the D flip-flops in the bidirectional shift registers for an 8-bit ADC, utilizing the proposed segmented DAC architecture. The obtained Signal to noise distortion ratio (SNDR) for the 8-bit ADC system is 55.73 dB, with the band of interest as 220 kHz and Effective number of bits (ENOB) of more than 9 bits.

Index Terms: *smart dust, continuous-time (CT), Delta modulation, Analog-to-digital converter (ADC), Digital-to –analog converter (DAC)*

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1. INTRODUCTION

The target of this paper is to study and design a mixed-signal processing system consisting of an Analog-to-Digital Converter (ADC), Digital Signal Processor (DSP) and Digital-to-Analog Converter (DAC), for the smart dust application, in a top-down, test-driven design methodology. The complete system has to be operated in a CT mode without any sampling. The focus is to achieve low power consumption and area, without sacrificing the overall system performance.

There has been a new phenomenon emerging out in recent past called "smart dust" also known as "motes" or "wireless sensor networks" or "swarming". Smart dust is a tiny (size and density of a sand particle), ultra-low- power electronic sensory autonomous device packed with various sensors, intelligence and even wireless communication capability. A typical scenario could be smart dust motes deployed in large numbers to form an ad-hoc network, called as swarm, detects environment variables such as light, temperature, pressure, vibration, magnetic flux density or chemical levels. This network, formed by few tens or even millions of motes, can communicate with neighboring motes and pass on the data collected from one mote to another in a systematic way, which can be collected and processed further [1]. Smart dust can derive the energy necessary for its functioning either from batteries or from the environment itself, or from both. The power consumption of the smart dust decreases with the shrinkage in the size of the mote. It has to be in the order of few microwatts. This imposes a stringent constraint on the design, and has to be addressed by following various low power design techniques.

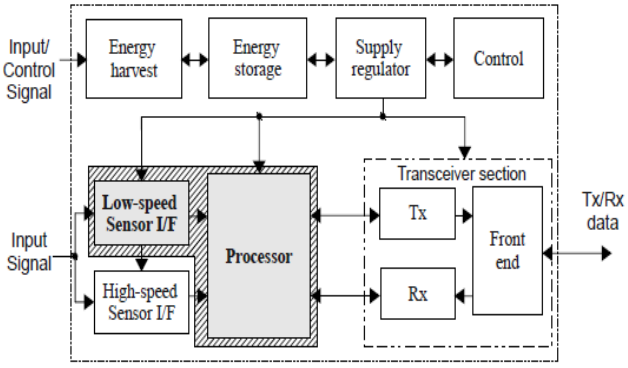

Fig- 1: Block diagram of a typical smart dust mote.

Fig-1 shows the block level details of a single autonomous smart dust supply regulator, control, high-speed sensor interface, low-speed sensor interface, DSP and radio transceiver section. Energy harvester generates energy from the environment such as solar radiation, wind or even vibration. The generated energy is stored for future usage, using an energy storage element. The

available energy is supplied efficiently, in the form of fixed voltages and currents, to the various circuits of the system with the help of the supply regulator. The control circuitry is responsible for the various control mechanisms involved in a mote, which decides the operation of the mote. The sensors collect the environmental variations of interest and convert them to an equivalent electrical signal, analog in nature. The sensory interfaces are required to perform initial signal conditioning and analog to digital conversion of the sensed data. The data is processed digitally using a DSP. DSPs can essentially perform various kinds of operations on the digital signals, such as filtering, domain transformations, compression, encryption, etc. The processed data is reconstructed back to analog equivalent necessary for transmission, using a DAC (not shown in figure). The transceiver section up-converts the baseband signal to Radio Frequency (RF) signals and transmits them. It also receives the RF signals and down-converts them to the baseband signal. This paper targets the design of the low speed sensor interface and the DSP, as highlighted in fig- 1.

The specifications of the CTDSP system, that is finally going to be deployed in the smart dust motes are shown in table 1. The major constraint imposed on the system is that all the blocks in the design should be clockless. Further, the system should be implemented in 90 nm advanced Complementary Metal Oxide Semiconductor (CMOS) process. The specifications of the ADC, DAC and the transversal direct-form Finite-Impulse-Response (FIR) Low Pass Filter (LPF) is as shown in table 1.

Table- 1 SPECIFICATIONS OF THE CT-DSP SYSTEM FOR SMART DUST

Item	Parameter	Value
ADC	Resolution	8 bits
	Maximum input signal frequency	20 KHz
LPF	Sampling frequency	44 KHZ
	Passband edge frequency	5.2 KHZ
	Stopband edge frequency	10KHz
	Pass band ripple	1 dB
	Stopband attenuation	50dB
DAC	Resolution	8
Generic	Supply voltage	1 V
	Technology	90nm

Continuous time processing

A new emerging field of digital signal processing in CT has been presented by Prof. Yannis Tsividis of Columbia University [2, 3]. It is opposed to the conventional sampled systems where the processing is carried out in discrete time. This CTDSP system processes the data sensed by the analog Interface block of the sensor module and produce the output to the RF front-end. As the input data is of burst nature, occurring occasionally, it is highly desirable that the CTDSP system remains idle most of the time and operates only when there is a significant data to process. This is achieved by using level crossing technique, where the ADC operates only if there is a significant variation observed in the input signal. It doesn't produce a sample if there is a long silence or no data available to process.

A conventional DSP system operates with a global reference or clock signal. The input signal, x(t), is sampled-and-quantized at the rising or falling edge of the clock signal for an edge triggered system. The quantized signal is encoded digitally and processed by the subsequent DSP section and the reconstruction of the digital signal to the analog equivalent by the output DAC.. The overall system is completely synchronized with respect to the global clock. The drawbacks of the conventional DSP systems are, A sampled system requires clock generator, which has a large fan-out, since it has to drive gates of many transistors. Hence, making it costly to implement both in terms of the area and power consumption, the sampling frequency is decided based on the highest frequency component of the input signal. It is therefore necessary to implement a band-limiting filter known as an anti-aliasing filter, to avoid aliasing, whose implementation might also be a costly affair, the sampling results in the aliasing of higher frequency terms to the band of interest, even if the Nyquist theorem is followed and the deviation from the precise sample timing instances due to the clock jitter and the clock skew can cripple down the system performance to undesired levels, if not designed properly.

The signal to be processed by the smart dust module is of burst nature, which occurs occasionally. The clocked systems, although equipped with many advantages, are not an ideal choice for processing the burst-like signals. The drawbacks listed for the clocked system are more dominating compared to the advantages for the smart dust application. Hence in this paper the event-driven CT digital signal processing systems are discussed, which operates on the principle of level-crossing and are very suitable for burst-type data processing.

2. CONTINUOUS-TIME OR EVENT-DRIVEN DSP SYSTEMS

The CT or event-driven Digital Signal Processor (DSP) systems, as the name suggests, operates in continuous time mode [2,6]. The input signal, x(t), is processed by the CTDSP system to produce output, y(t). There is no clock involved anywhere in the system. A CT system can also be divided into three basic sub-systems: the CTADC, CTDSP and CTDAC. As pointed out above, there is no global clock involved anywhere in CTDSP system. Hence, all the three blocks operates in a CT mode and are represented with a prefix CT [5]. Figure 2 shows the block diagram of the CTDSP system with the three sub-systems. CTADC is the first block in the CTDSP system which quantizes and digitizes the input signal, x(t), to a CT output, bi(t). Unlike conventional system, the input signal is not sampled before quantization. The CT data is then processed by the CTDSP sub-system to produce digital data, dj(t), which is reconstructed to analog signal, y(t), by the CTDAC block. Note that the time domain is represented in "t" as it is always continuous in nature.

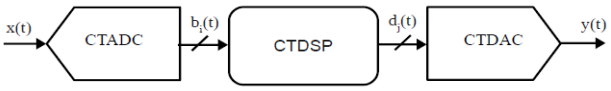

Fig- 2: CTDSP system with the basic building blocks CTADC-CTDSP-CTDAC.

The CTDSP system adopts non-uniform sampling approach, where samples are generated only when the event crosses predefined quantization reference level. The operation of the CTDSP system can be classified as quantization by the CTADC block and the processing of the digital (continuous) data by the CTDSP subsystem.

2.1 CTDSP QUANTIZATION TECHNIQUE: A LEVEL-CROSSING APPROACH.

A conventional DSP system adopts uniform quantization technique, where samples are taken and processed at every clock cycle. The maximum frequency of the input signal dictates the minimum possible clock frequency of sample generation. However, it turns out that, for signals with burst-like nature and long period of silence, exhaustive sampling is not required as done in conventional systems. The samples generated either contains no information or repetitive information. Further, additional dynamic power is required for the processing of these samples by the DSP section. A different class of the quantization technique, called a level-crossing sampling scheme, suggested by Sayiner et al., and further explained by Tsividis in [2, 3, 5]. It is a non-uniform sampling approach, where the samples are generated only when the event crosses the predefined quantization reference level. Since the quantization is based on the event and is continuous in time, it is called as an EDCT quantization [3].

The quantization steps can be uniform or non-uniform and can be customized further based on the application. To understand the CT quantization technique, let's consider figure.3. As shown, the input signal, x(t), when crosses the predefined quantization reference level, get quantized to signal, xq(t), and produces samples (ti, x(ti)). This is a non-uniform sampling operation, where the signals with faster slope generate samples more frequently ("faster") compared to signals with lesser slopes. Hence, signal-dependent sampling is achieved simply by utilizing the built-in feature of the quantizer. With this approach, the signal with less variation produces lesser number of samples to be processed by the subsequent DSP section; hence resulting in a signal dependant power consumption. This is a clear advantage of the CT systems, making it very suitable for processing burst type signals.

The continuous-time digital output, bi(t), of the CTADC block is processed by the CTDSP sub-system. Since the ADC output is digital in nature, the advantages of the digital signal processing can be utilized in the CT system as well. The design approach for the CTDSP system is described in [6]. Based on the transfer function, a conventional DSP system can be realized using multipliers, adders and delay taps as basic building blocks. A digital signal processor operating in the CT mode can be mapped from the discrete counterpart by replacing these blocks by the one operating in the CT domain. For Example, asynchronous multipliers and adders, which operates without clock, can be used in the CT system. One method of implementing the delay taps is by using chain of inverters. A better approach is presented in [9,10], where collection of delay cells connected in series are used to delay and hold the data. Handshaking is used between delay cells to ensure proper data transmission. The usage of these delay blocks are experimentally confirmed in [4, 11]. The CTDSP sub-system produces output, dj(t), as shown in fig- 2, which is reconstructed back to the analog equivalent, y(t), by the CTDAC module. The CTDAC can be realized using architectures and circuit implementation techniques as mentioned in section V for the clocked counterpart. The only difference is that the DAC should operate without clock.

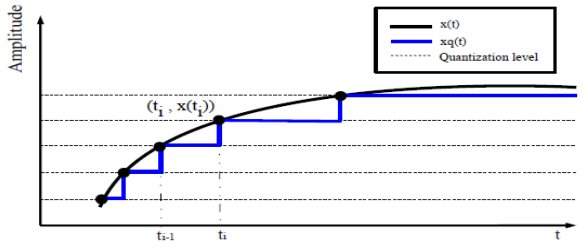

Fig-3: Level-crossing quantization technique in CTDSP system

3. EVENT-DRIVEN ADC

The first module in the ED DSP system is the CTADC or the ED ADC. It converts the analog input signal, x(t), provided by the Analog Interface (AI) to CT digital binary output signal, bi(t). A block diagram of the AI and the CTADC is shown in figure 4. The AI section consists of a sensor network and an analog filter. The sensor network detects the variation in the input signal (temperature, pressure, humidity , etc. based on the application) and converts it to the electrical signal. The analog filter limits the frequency of the input signal to the operating range of the ADC.

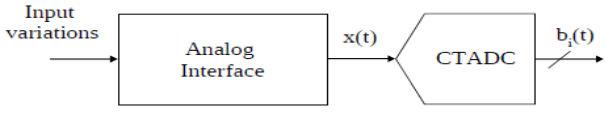

Fig- 4: Block diagram of AI and CTADC.

The AI is designed based on the overall specification defined for the smart dust module, for e.g., the sensor interface is selected based on the application and the cutoff frequency of the analog filter is selected based on the frequency of operation of the system. As illustrated in figure 4, the AI provides a CT signal,

x(t), to the CTADC block. The CTADC consists of a CT quantizer and an encoder, which digitize the signal to, bi(t). The digital output, bi(t), is continuous in time and can be represented in many ways depending on the deployed ADC architecture [3].

3.1 LEVEL-CROSSING SAMPLING FOR THE CTADC

The CTADC adopts a level-crossing sampling technique. In this section a detailed description of the level-crossing quantization technique is presented. Figure. shows the quantization procedure in the CTADC. When the input signal, x(t), crosses a quantization reference level, it gets quantized to the nearest quantization level based on the direction of the input signal. The quantized signal, xq(t), as shown in figure 5, is continuous in time and the samples are represented as (ti, x(ti)), where ti−1 and ti represent the time instances of the sample generation, respectively. The quantized signal, xq(t), can be digitized in many ways [3], like the CT binary bits in a flash ADC or by using data token consisting of change and direction (increment/decrement) as in DM [15]. The former approach is illustrated in figure.5, where b0, b1 and b2 are the CT binary signals. The level-crossing sampling is a non-uniform sampling operation, where the faster signals with higher slopes generate samples more frequently ("faster") compared to signals with lower slopes. Hence, a signal-dependent sampling is achieved simply by utilizing the built-in feature of the quantizer. It means that an input signal with lower variation generates lower number of samples to be processed by the subsequent DSP section, hence achieving lower dynamic power dissipation.

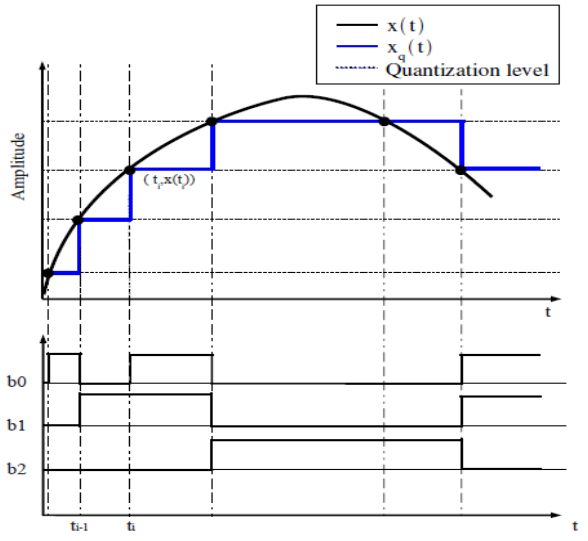

Fig- 5: Level-crossing quantization in the CTADC with 3-bit CT digital output representation; b0, b1 and b2.

The frequency spectrum of an 8-bit CT quantizer as well as the sampled quantizer is shown in figure 6 and fig-7, respectively. The CT quantized signal spectrum has only the signal and its harmonic components. Whereas, the output spectra of the conventional sampled quantizer contains not only the signal and its harmonics, but also other undesirable tones, which are spread across the entire spectrum, and are not harmonically related to the signal frequency. This is an artifact due to aliasing of the higher frequency harmonic distortion components into the lower frequency band of interest and can be attributed to the sampling of the CT quantized output, which is just same as the conventional technique of quantization after sampling. Hence the difference between fig-6 and fig-7 is the noise floor added in the latter case due to aliasing, which is an inherent feature of sampling.

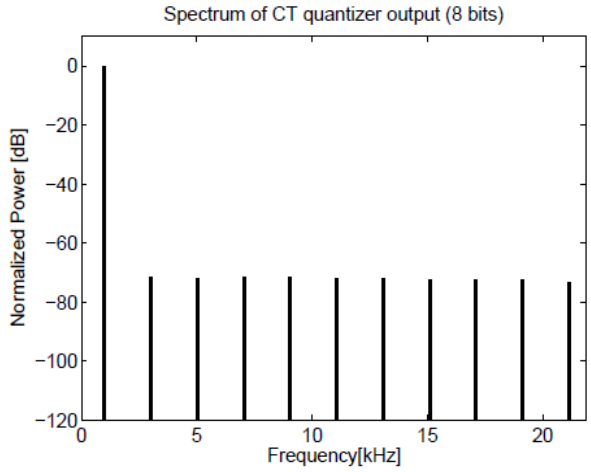

Fig- 6: Frequency spectrum of an 8-bit CT quantizer with input amplitude A = xmax.

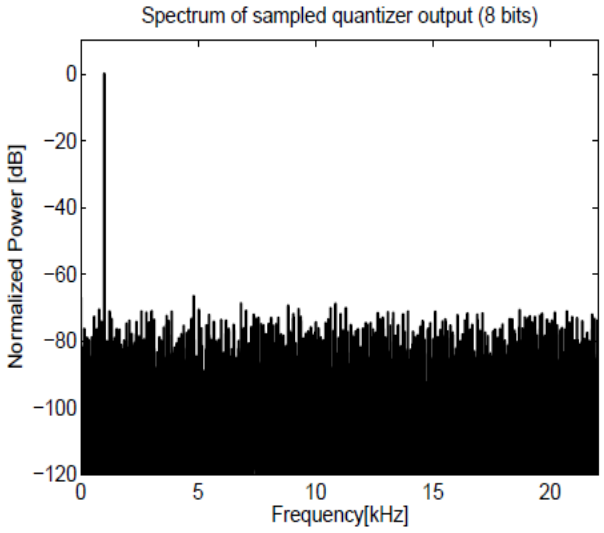

Fig-7: Frequency spectrum of an 8-bit sampled quantizer with frequency of sampling, fs = 44 kHz.

3.2 PROPOSED ARCHITECTURE OF AN EVENT DRIVEN DM ADC

An ED DM ADC system consists of two comparators, a feedback DAC, a bidirectional Shift Register (SR) and an asynchronous digital control logic. The block diagram of the ED DMADC system is shown in figure.8. The DAC generates two reference signals: VTop(t) and VBot(t) for the upper and lower comparator, respectively. The upper (lower) comparator tracks the positive (negative) going signal and produces output Inc (Dec), which is high, when input signal is greater (lesser) than VTop(t) (VBot(t)) and zero when the signal is in between the two reference levels. Based on the value of Inc/Dec, the digital asynchronous control logic produces signals: change and direction, collectively called as "data token ". The data token is provided to the bi-directional SR which increments (decrements) the DAC outputs, VTop(t) and VBot(t), by _ (voltage resolution of the ADC), if Inc (Dec) is high. The data token is also provided to the subsequent DSP section, which processes the samples. The DSP section sends the acknowledge signal Ack back to the control logic.

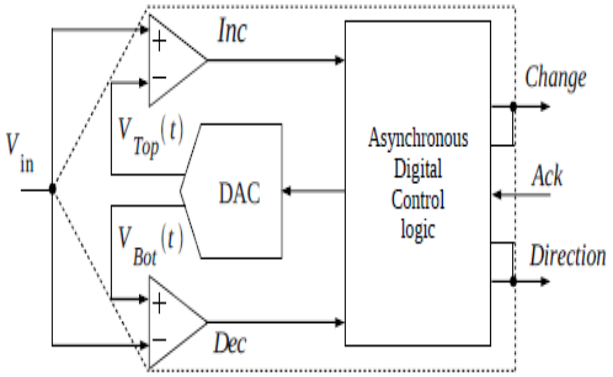

Fig-8: Event-driven ADC based on delta modulation technique.

4. CONTINUOUS TIME DSP

After the CT quantization of the input signal picked up by the sensor, to infer the information content of the quantized and digitized tokens, one has to process it. The processing is done using a digital signal processor, before the data transmission. This can be performed either in CT or discrete-time. The CTDSP is preferred over the conventional sampled DSP, to avoid sampling clock and the drawbacks associated with it. CTFIR filter is considered for designing the CTDSP. The CT processing of the signals in digital domain can be achieved by using basic blocks such as adders, multipliers and delay elements, all operating in continuous mode. The subsequent discussion provides detail about the design of
the DSPs system operating in CT.

4.1 EVENT-DRIVEN FIR FILTER WITH DELTA MODULATION TECHNIQUE

An approach is to use an asynchronous DMADC. The two signals which collectively form the output data token from the DMADC are change and the direction. The change represents the time instance of the sample generation and the direction represents the sample value which can be "high" or "low". Note that, these two binary signal fully represents an N-bit signal and can be reconstructed back to the quantized signal, q(t). Henceforth, change and direction are collectively called as a data token ([change, direction]). As shown in fig- 9, the data token is passed to the up-down counter, which counts up or down by 1 LSB if the data token is [1,1] or [1,0], respectively. Counting up or down can simply be performed by adding or subtracting 1 LSB from the previous value stored in the counter. The output from the counter is q(t − k.TD), which is multiplied with the tap coefficient, bk, to produce output, mk(t), as given by

$$mk(t) = bk \cdot q(t - k \cdot TD). \qquad (1)$$

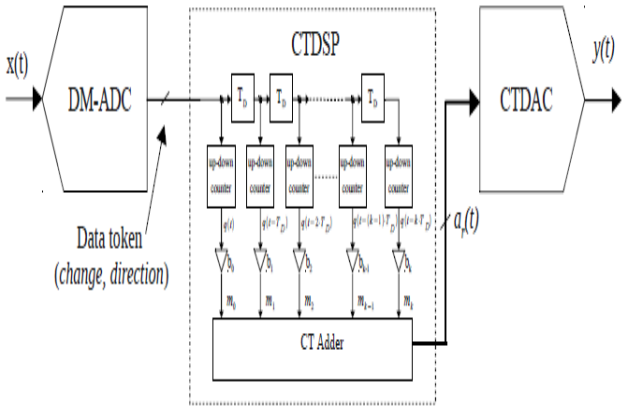

Fig-9: Event-driven FIR filter with DM encoding technique.

And the final output, y(t), which is the weighted sum of mk(t), is given by

$$y(t) = \sum_{k=0}^{K} m_k(t) = \sum_{k=0}^{K} b_k \cdot q(t - k \cdot T_D). \qquad (2)$$

4.2 DESIGN CONSIDERATION OF CTDSP SYSTEM

In this section a few basic design parameters are discussed that are required for designing the CTDSP system. A transfer function of the CTDSP system is the filter transfer function, B(s), can be determined by taking the Laplace transform of output, y(t), as given by equation (2), where y(t) is represented as the linear combination of the quantized input signal, q(t). The output Y (s) of a system with frequency response, B(s), and a quantized input signal Q(s) is given by

$$Y(s) = Q(s) \cdot B(s). \quad (3)$$

The expression for Y (s) can be written as

$$Y(s) = [\sum_{k=0}^{K} b_k \cdot e^{-s \cdot T_D \cdot k}] \cdot Q(s). \quad (4)$$

The data token generated by the CTADC depends on the slope of the input signal. The total number of data tokens generated and the minimum possible distance between the two tokens are of primary importance, as it defines the functional requirement on the DSP section. Both, the number and the distance between the two data tokens has to be preserved, to achieve the correct filtering operation by the DSP block. Any missing data token or deviation in the distance between the two tokens, may result in undesirable variation in the frequency response of the filter.

The CTADC should be able to operate at the rate of 1/Tmin, which for the above case of fb= 20 kHz is approximately equal to 16 MHz. This is equivalent to oversampling the ADC by a rate of 400. Hence, this system is suitable only for low frequency operation, because, for the high input frequency and considering the same oversampling ratio, the data token rate goes drastically high, which can be impractical for implementation with the mainstream CMOS process. Based on the above discussion and design parameters, fb and N of the ADC, it is possible to roughly define the power consumption of the CTDSP system.

5. CONTINUOUS TIME DAC

The CTDAC is the final block of the CTDSP system. It converts the digitally processed CTDSP sub-system output to an analog equivalent. In the previous sections, it is concluded that the DM-based ADC and DSP are preferred architectures for the smart dust application. Hence, the DAC architecture selection is based on the assumption that it is capable of accepting the 8-bit output word from the DM operated DSP sub-system. Also, as shown in fig-8, one feedback DAC is required inside the CTADC block. Hence, there are two DACs in the complete system. Target of the design is to reuse the same architecture in both the places. Any DAC which work asynchronously can be used for this purpose.

Few important points to take care, while selecting the DAC architecture, which is suitable for the feedback as well as the output DAC, are: The CTDAC shall generate two reference levels VTop(t) and VBot(t) required as a reference for the top and bottom comparators shown in fig-8. The two reference levels are separated by ΔLSB given by equation (2)

$$VTop(t) - VBot(t) = \Delta LSB. \quad (2)$$

Note that this constraint is not applicable for the output DAC, where only one output is required. The output shall increment or decrement by only one bit at a time to track the input signal continuously in the DMADC. It shall operate in an asynchronous mode without any clock, as no clock is used in the other sub-modules. It shall occupy very less area and it shall consume as less power as possible.

There are many possible architectures which can be used for realizing the required DAC structure with the constraints given above, e.g., resistor-string (R-string), current steering DAC, charge accumulation DAC and segmented DAC [7]. It has been shown in [11], that a resistor-string DAC architecture occupies lesser area, consumes less power, simple in design and can generate the two reference levels as described above. Due to these advantages a resistor-string DAC architecture is selected in this design.

5.1 SEGMENTED RESISTOR-STRING DAC

It is described that the resistor-string DAC architecture is preferred over the other DAC architectures. However, the simple resistor-string DAC may not be a cost effective solution for higher ADC is to use segmented resistor-string architecture, which produces same resolution as resistor-string architecture, with less hardware. Various possible segmented DAC architectures are available with the advantages and drawbacks. A final DAC architecture is presented, which is used in the design and block diagram is shown in fig- 10.

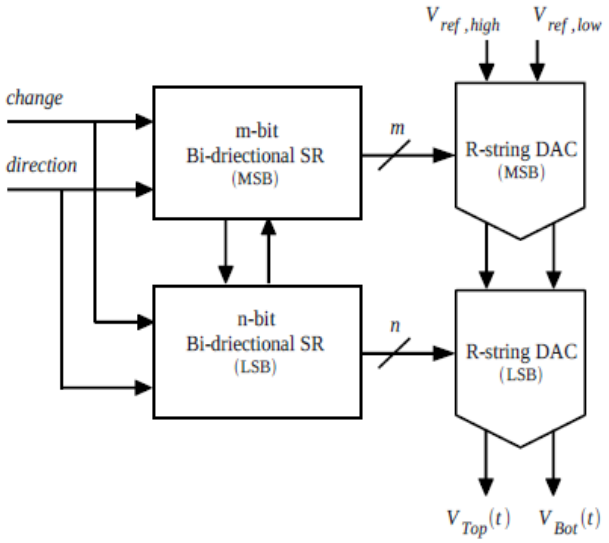

Fig- 10: Block diagram of the m × n segmented resistor-string DAC with the m × n segmented bi-directional Shift registers.

The segmented m × n resistor-string DAC consists of two segments, where the first string with m resistors, resolves the Most Significant Bits (MSBs) and the second substring with n resistors, resolves the Least Significant Bits (LSBs) [7].

As shown in fig-10, two bi-directional SRs are required in this architecture, which based on the data token, produces m and n bit control signals for the MSB and LSB string, respectively. One possible selection of m and n is given by

$$m = \begin{cases} n = 2^{N/2}, & if\ N\ is\ even \\ n/2 = 2^{(N-1)/2}, & if\ N\ is\ odd. \end{cases} \quad (5)$$

Fig-11 presents the segmented resistor-string DAC architecture with the MSB and LSB strings. Vref,high and Vref,low are the highest and lowest output reference voltages, respectively, from the DAC and are applied across the MSB string. The control signals, m and n from the bi-directional SR, are applied to the switches used to tap the output of the MSB and LSB string, respectively. Only one output is high at a time for each m and n bits. The total number of resistors in the segmented DAC and the total number of flip-flops in the bi-directional SR are now given by (m+n) and the total switches in the DAC are given by (2) · (m+n). The voltage step, ΔMSB, resolved by each resistor in the MSB string is given by

$$\Delta_{MSB} = \frac{V_{ref,high} - V_{ref,low}}{m}, \quad (6)$$

which is further resolved by the LSB string to voltage step, Δ, given by

$$\Delta = \frac{V_{ref,high} - V_{ref,low}}{m \cdot n}, \quad (7)$$

where m·n = 2N. Hence, the segmented architecture produces the same resolution as obtained by an N-bit resistor-string DAC, with reduced hardware count.

This architecture, however, suffers from the loading effect of the LSB string to the tapped MSB resistor as explained next. Let RMSB and RLSB be the respective resistances of each resistor in the MSB and the LSB string. The total series resistance of LSB string, RLSB,T otal, is given by

$$\text{RLSB,T otal} = \text{n.RLSB}. \quad (8)$$

The equivalent resistance, RMSB, Equivalent, of the tapped MSB resistor in parallel to RLSB,T otal is given by

$$\text{RMSB,Equivalent} = \text{RMSB} \parallel (\text{n.RLSB}), \quad (9)$$

which is different from RMSB. Hence, the voltage drop across the tapped MSB resistor is not exactly equal to ΔMSB, as given by equation (6). It results in the generation of incorrect reference voltages at the output of the DAC. The loading effect of the LSB string to the MSB string can be avoided simply by adding buffers between the MSB and the LSB string then

$$\text{RMSB,Equivalent} = \text{RMSB}. \quad (10)$$

It means, that effectively there are m resistors in series in the MSB string, with each resistor generating ΔMSB as given by equation (6), which is exactly the same as required. Hence, with the proper choice of LSB string resistors, the loading effect can be avoided.

6. SIMULATION RESULTS

Systematic top-down test-driven methodology is employed throughout the project. Initially, MATLAB models are used to compare the CT systems with the sampled systems. The complete CTDSP system is implemented in Cadence design environment. The architecture of the DM ADC system ,as shown in Fig.8. is used to realize a high level working model of an 8-bit ADC system employing the proposed segmented DAC architecture.

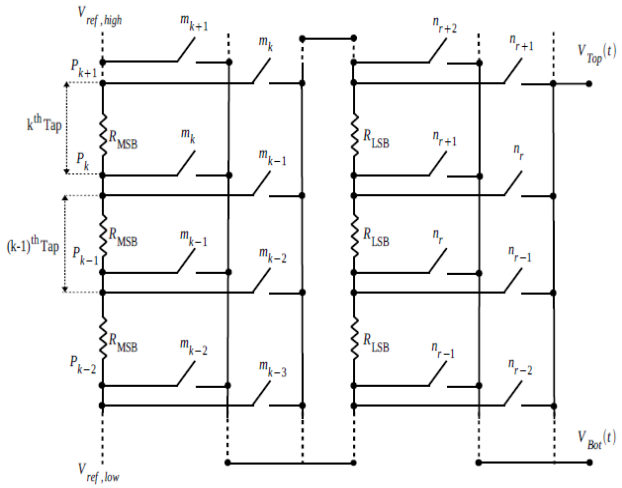

Fig- 11: Resistor-string segmented DAC architecture.

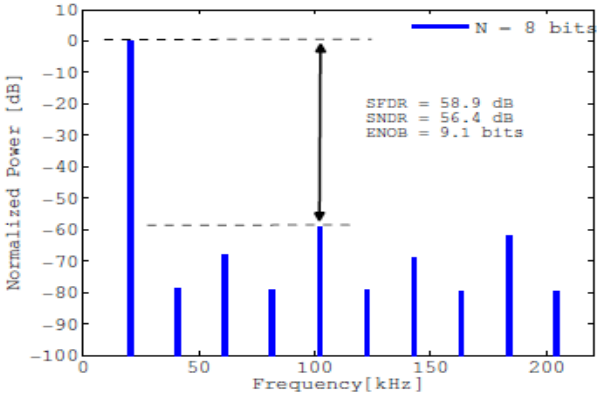

Fig- 12: Output frequency spectrum of an 8-bit DM ADC with 16×16 shared MSB resistor DAC, 20.416 kHz input frequency and 220 kHz band of interest.

Table II. Comparision of components, SNDR and ENOB obtained for 8-bit system for different types of DACs.

Parameter	8-bit ADC with Resister string DAC	8-bit ADC with Segmented-Resister-string DAC
Frequency band	220	100
SNDR(dB)	56.5	67.5
ENOB	9.1	10.9
Resisters in DAC	512	64
Switches in DAC	256	33
D Flip-flop in DAC	256	32

The noise immunity to the system is provided by adding an offset of Δ/4 to the lower comparator of the CTADC. The system is tested with an input sinusoid of frequency 20.416 kHz, the SNDR obtained for the 8-bit system is around 56.5 dB when considering the band of interest as 220 kHz. For the smart dust application, a resolution as high as 8-bit is not required. It is possible to reduce the number of bits to 3-bits and still be able to detect the signal at the input and process it.

The fig-12 presents the spectrum of an 8-bit ADC system plotted . It can be observed that the odd order harmonics are dominating in the spectrum and even order harmonics are suppressed by more than 80 dB. Hence no noise floor.

Table II presents a comparison of the SNDR and ENOB for an 8- bit ADC using resister string DAC and 8- bit ADC using segmented resister string DAC. The SNDR improvement can be observed when the band of interest is reduced from 220 kHz to 100 kHz and improvement of ENOB is also clearly observed.

It has been shown that the sensitive feedback DAC or resistor string DAC used in the ADC can be modified further to a segmented structure, which helps in reducing the overall components(resistors, switches, and D Flip-flops) observed is approximately 87.5%. in the design. The savings are doubled for systems utilizing similar DAC at the DSP output.

The hardware overhead for ADC system utilizing the proposed segmented architecture reduces drastically compared to the ADC using resistor string DAC. Hence, it is possible to design an N-bit ADC with a segmented DAC architecture which utilizes lesser hardware compared to its resistor string counterpart and provides better performance.

The transient response of the 8-bit system with 8-bit ADC, 8-bit DSP and 8-bit output DAC with 20.4 kHz input frequency. The overall output of the system is shown on the right side of the figure, OutChange and outDirection are the tokens generated by the digital delta modulator.

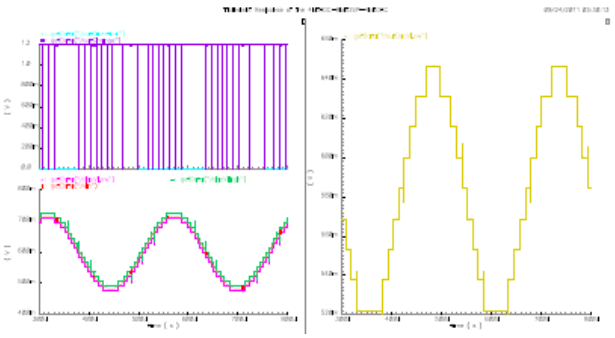

Fig-13: Transient response of the 8-bit system with a 8-bit ADC,8-bit DSP and 8-bit output DAC and 20.4 kHz sinusoidal input frequency.

CONCLUSIONS

This paper presents Continuous time ADC and DSP system for smart dust and wireless applications it is concluded that the CT processing is very well suited for the smart dust application. The noise immunity to the system is provided by adding an offset of Δ/4 to the lower comparator of the CTADC.

To validate the presented theory, an 8-bit ED ADC system is designed. It has been shown that the sensitive feedback DAC used in the ADC can be modified further to a segmented structure, which helps in reducing the overall components in the design. The Lower SNDR obtained for the 8-bit system as there is no noise present in the output spectrum.

The presented system CTADC or the ED ADC and CT DSP section can be potential area and energy saver and its suitability for smart dust and wireless applications is shown.

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