FIRST ORDER SIGMA-DELTA MODULATOR WITH LOW-POWER CONSUMPTION IMPLEMENTED IN AMS 0.35 µM CMOS TECHNOLOGY

RADWENE LAAJIMI

NIZAR KHITOUNI, University of Sfax, Department of Electrical Engineering Electronics, Micro-technology and Communication (EMC) research group Sfax (ENIS), BP W, 3038 Sfax, Tunisia
radwene_fac@yahoo.fr

Abstract

This paper presents a design of a switched-capacitor discrete time 1st order Delta-Sigma modulator used for a resolution of 8 bits Sigma-Delta analog to digital converter. For lower power consumption, the use of operational transconductance amplifier is necessary in order to provide wide output voltage swing and moderate DC gain. Simulation results showed that with 0.35um CMOS technology, 80 KHz signal bandwidth and oversampling rate of 64, the modulator achieved 49.25 dB Signal to Noise Ratio (SNR) and the power consumption was 5.5 mW under ±1.5V supply voltage .

Index terms: *Analog-to-Digital conversion, Delta-Sigma modulation, CMOS technology, Transconductance operational amplifier.*

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1. INTRODUCTION

Sigma-Delta (ΣΔ) Analog to Digital Converters (ADC) [1] has been successful in realizing high resolution consumer audio products, such as MP3 players and cellular phones for some time now. DS converters are well suited for low bandwidth, high-resolution acquisition, and low cost, making them a good ADC [2] choice for many applications. ΣΔ [3] converters combine an analog ΣΔ modulator with a more complex digital filter.

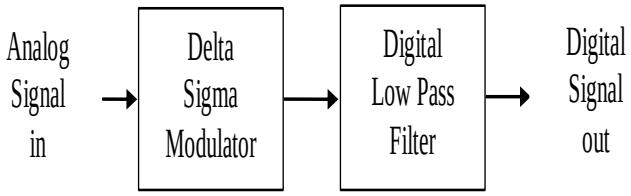

Figure 1: Block diagram of the ΣΔ analog to digital converter

Accuracy depends on the noise and linearity performance of the modulator, which uses high performance amplifiers. ΣΔ modulators trade resolution in time for resolution in amplitude such that the use of imprecise analog circuits can be tolerated. The narrow bandwidths in digital audio applications have made oversampled converters particularly appealing.
A block diagram of an analog to digital converter using ΣΔ modulator is shown in Figure 1. ΣΔ converters come into the category of oversampled converters. Oversampling is simply the act of sampling the input signal at a frequency much greater than the Nyquist frequency. One significant advantage of the method is that analog signals are converted using only a 1-bit ADC and analog signal processing circuits having a precision that is usually much less than the resolution of the overall converter. The penalty paid for the high resolution achievable with ΣΔ is that the hardware has to operate at the oversampled rate, much larger than the maximum signal bandwidth, thus demanding great complexity of the digital circuitry. First-order ΣΔ modulator has the advantages of being simple, robust and stable. This modulator is shown in Figure 2.

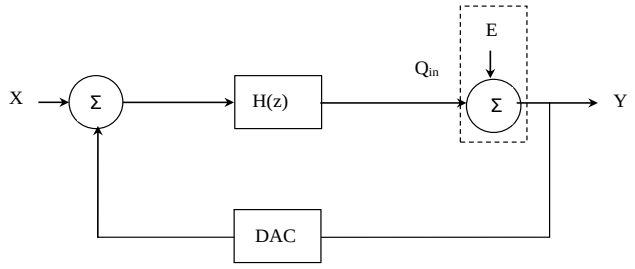

Figure 2: Linear model of first order ΣΔ Modulator

The modulator can be considered as a two-input, one-output linear system. The signal transfer function, STF(z) of this system is:

$$STF(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)} \quad (1)$$

And the noise transfer function, NTF(z) is:

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} \quad (2)$$

By using superposition principle, the output signal is obtained as the combination of the input signal and the noise signal, with each being filtered by the corresponding transfer function:

$$Y(z) = STF(z).X(z) + NTF(z).E(z) \quad (3)$$

By properly selecting the loop filter, the signal transfer function and the noise transfer function of a theoretical 1st order ΣΔ modulator yield in the z-domain:

$$STF(z) = z^{-1} \quad (4)$$

$$NTF(z) = (1 - z^{-1}) \quad (5)$$

Solving (1) and (4) gives:

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \quad (6)$$

Note that loop-filter is simply an integrator which can be easily implemented with switched-capacitor techniques. For a generalized Lth order ΣΔ modulator, the transfer functions become:

$$STF(z) = z^{-L} \quad (7)$$

$$NTF(z) = (1 - z^{-1})^{L} \quad (8)$$

To achieve a transfer function of Lth order, L basic building blocks i-e L integrators are required. When the modulator order is higher than one, the frequency response of NTF presents the characteristic of high-pass filters. The higher the order L is, the more quantization error energy is suppressed at low frequencies.

In this way, the output signal for the ideal linear model can be written as:

$$Y(z) = X(z).z^{-L} + E(z).(1 - z^{-1})^{L} \quad (9)$$

Analog to Digital Converters (ADC) as the interface of analog circuit and digital circuit connection, which is widely used in various systems and is a very important module. But the DS uses rate to substitute accuracy and reduce the performance requirement of the circuit, which is an effectively way to achieve high-precision ADC [4]. Discrete time ΣΔ modulator [5][6] significantly reduces the requirements of the operational amplifier gain and noise by using well capacitive matching characteristics, oversampling and noise shaping technology, so it is very suitable for the application of low voltage.

The main objective of a receiver for wireless communication applications is to recover the base band signals that are modulated on a carrier wave at radio frequencies. The design of a high performance, low power integrated radio frequency receiver in mainstream silicon technologies CMOS is a very challenging task involving numerous tradeoffs during the design process, especially between noise, linearity and power consumption.

To achieve the objective cited above, all aspects of the receiver [7] and radio system need to be addressed as shown in table 1. (Base band, Modulation scheme, hopping bandwidth, data rate)

Table 1: Sensor receiver specifications

Direct conversion receiver	
Base band frequency (fb)	80 Khz
Modulation scheme	BFSK
Hopping bandwidth	7 MHz (863-870) MHz
Data rate (D)	20 Kbps

The paper is organized as follows. Section II presents the proposed structure of the ΣΔ modulator with simulations results. In section III, all main parameters of the described modulator are indicated with a full comparison of the most popular designs in which the performance of each modulator is cited in table 4. Conclusion is drawn in Section IV.

2. PROPOSED STRUCTURE OF THE DELTA-SIGMA MODULATOR

First order ΣΔ modulators are probably the most common category of the device which has more stability than second order and third order circuit. At the core of any ΣΔ modulator lie integrators; they are usually implemented in CMOS technology. First-order ΣΔ modulator has the advantages of being simple, robust and stable. If we compare first order ΣΔ modulator with the other types in terms of power consumption and size they consumed low power.

The effective number of bits of ΣΔ (Neff) converter is given by [8]:

$$N_{eff} = \frac{1}{2}\log_2\left[(2N-1)^2(2L+1)\,OSR^{2L+1}/(\pi)^{2L}\right] \quad (10)$$

Where N represents number of bits of the quantization circuitry (N = 1), L represents order of modulator (L = 1) and OSR means Over Sampling Ratio which is based on the following formula:

$$OSR = \frac{F_s}{2\times f_b} \quad (11)$$

If we choose an OSR equal to 64, Fs is the sampling frequency which is calculated to 10.240MHz, and fb means base band frequency (80 KHz). The number 8.14 bits is the theoretical number because errors in the structure of parasites modulator reduce the SNR and therefore the number of bits, and to ensure low power and minimum consumption the number of bits is chosen as 8 bits.

The functional diagram of the first order modulator simulated using Simulink in MATLAB is shown in Figure 3. The single bit DAC is replaced by a simple wire. The input is a sinusoidal signal with 0.4 V amplitude and frequency 20 kHz. This signal is fed through only one integrator and is connected to the comparator at the output.

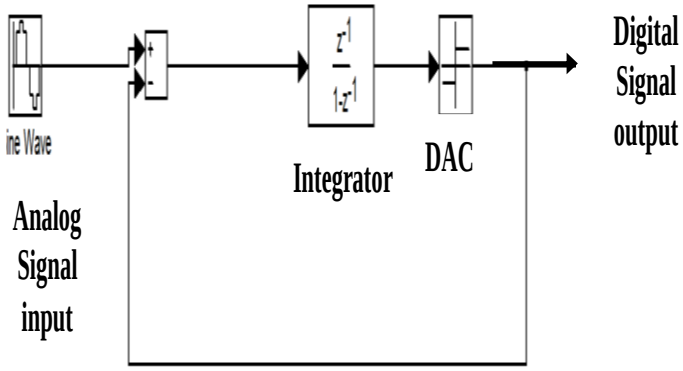

Figure 3: Block diagram of First Order ΣΔ Modulator

The modulated output as seen through the scope is shown in Figure 4 with the input signal overlaid on it.

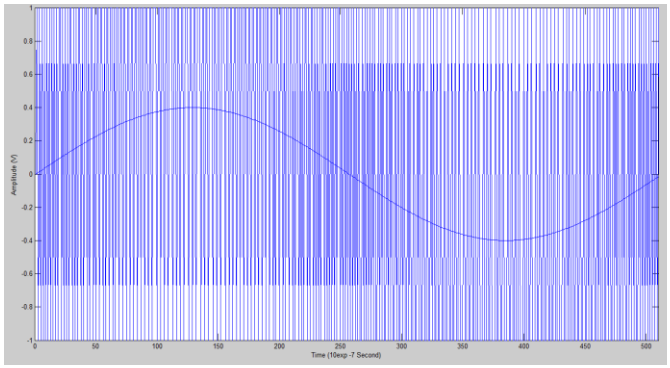

Figure 4: Block diagram of First Order ΣΔ Modulator

A discrete Fourier Transform (DFT) of the sampled output signal is performed to calculate the SNR of the system. The logarithm of the amplitude of the signal is plotted versus the signal frequency and the SNR is found to be close to 49.25 dB as shown in Figure 5.

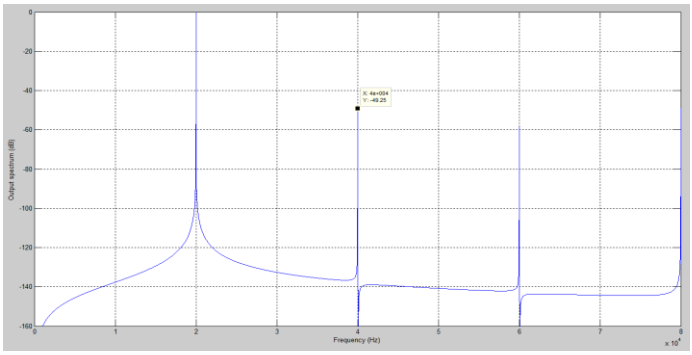

Figure 5: Frequency spectrum zoom of the modulated signal

It can be seen that second order noise shaping is taking place wherein most of the noise is pushed to the higher frequency bands as shown in figure 6. The original signal can be retrieved using a digital low pass filter.

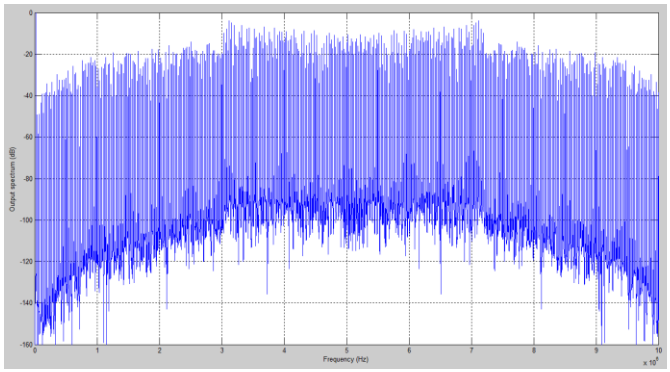

Figure 6: Frequency spectrum of the modulated signal

Figure 7 shows a block diagram of a complete first-order ΣΔ modulator. It is made up of only one integrator, a comparator, and digital to analog converter (DAC). These include switches Q and Q' for applying one of two reference node voltages, +Vref and -Vref, depending on comparator output polarity. The integrator is based on amplifier, and use two phase, with the respective phases denoted by Φ1 and Φ2.

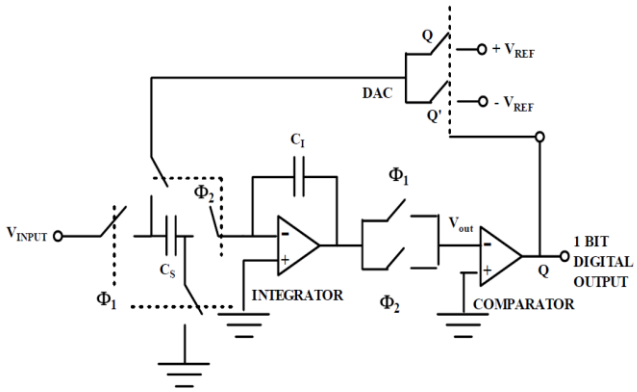

Figure 7: A complete first-order ΣΔ modulator

It is important that an Operational Transconductance Amplifier (OTA) intended for insertion into a ΣΔ modulator have an adequate bandwidth and a sufficiently high voltage gain at the lower frequencies, because the former property determines the modulator bandwidth, and the latter makes for lower quantization noise.

The circuit diagram of OTA [9] with modified current source shown in figure 8, contains two input transistors formed by P-channel MOSFETs M1 and M2. Either N-channel MOSFET (NMOS) or P-channel (PMOS) input devices can be used. However, PMOS input devices are used more often thanks to improved slew rate and reduced 1/f noise [10]. The use of PMOS input devices also provides reduced power supply rejection thanks to the current mirrors, and low sensitivity to change in power supply voltage. This first stage of op-amp also had the current mirror circuit formed by an N-channel MOSFETs, M3 and M4. The transistor M7 serves as an P-channel common source amplifier which is the second stage of op-amp. The architecture of modified current source is composed of two blocks: polarisation and correction.

The polarisation block is formed of four transistors (M12, M13, M14, M15) with variable input voltage Vin and input resistance Rin. The correction block is composed of three transistors (M9, M10, M11).It characterized by minimum error of copying accuracy due to the equality of drain source voltage between M10 and M11.This equality thanks to an amplifier between the mirror's input and output transistors M10 and M11 and causes high accuracy and good linearity. High output impedance is obtained by the output current of amplifier and passes to the gate of transistor M9. In order to achieve high current copy accuracy, it is necessary to use an amplifier between the mirror's input and output transistors.

The architecture of this amplifier architecture is created by K.Tanno[11]. As shown in figure 9, this structure is formed by only two NMOS transistors (MN1 and MN2) in which MN1 is operated in the weak version region (source gate voltage of MN1 equal to zero).This version can operate either in the linear region or in the saturation region for achieving low voltage and low consumption. Moreover, the conventional amplifier which has four transistors causes the increase of the power dissipation and the chip area. The advantages of the scheme proposed by K.Tanno are low voltage operation, small chip area, high output resistance and no bias current. For this reason we use this structure in voltage to current converter. The overall gain of the amplifier is found to be given by:

$$A_v = g_{m1}\left(r_{ds2} \,//\, r_{ds4}\right).\, g_{m7}\left(r_{ds6} \,//\, r_{ds7}\right) \qquad (12)$$

Where gm i is the transconductance and rds i is the drain to source resistance of i th transistors with i =1,2,4,6,7.

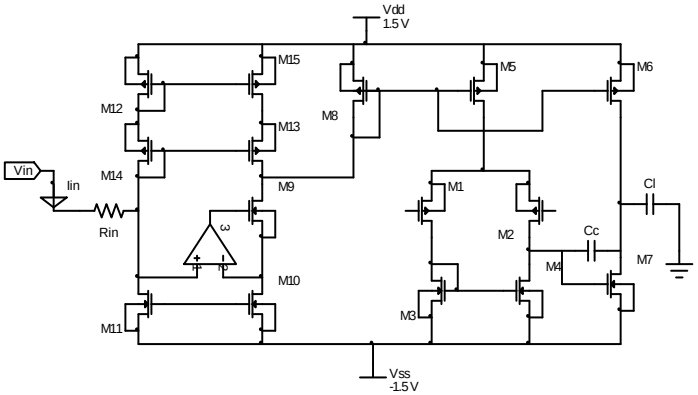

Figure 8: Operational Transconductance Amplifier with modified current source

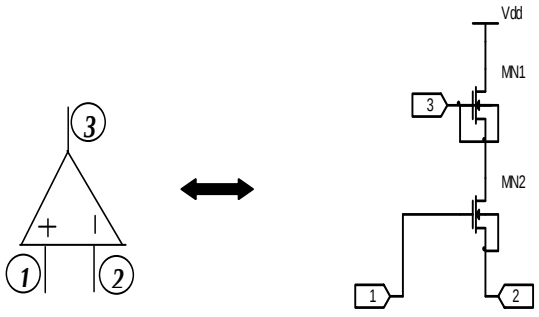

Figure 9: Two-transistor amplifier structure

Using Tspice based on BSIM3V3 transistor model for the technology 0.35µm at ±1.5V power supply voltage, the simulated output frequency response of our OTA is shown in

figure 10. The bode diagram gives an open loop gain of 60 dB with a large GBW of 82 MHz, a 97 KHz of cut-off frequency and a phase margin of 62°. We note that the input current passes through M8 using for polarisation are equal to 10µA and this corresponds to an input voltage Vin of -1V.

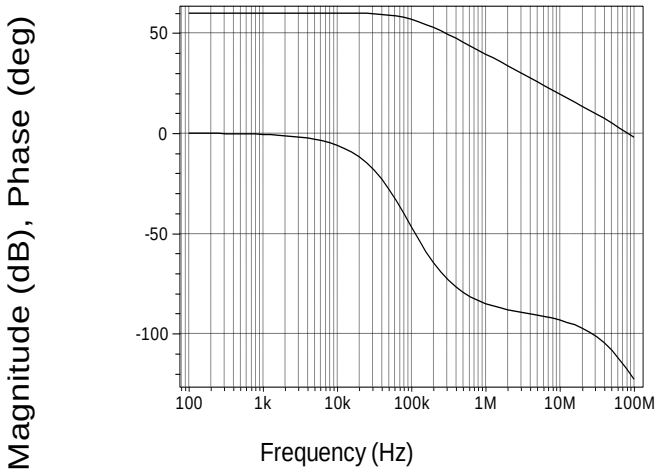

Figure 10: Frequency response of Operational Transconductance Amplifier

3. RESULTS AND COMPARISON

The modulator is designed using a 0.35um CMOS process, the over sampling ratio is 64 with a signal band width of about 80kHz.All main parameters of the described modulator are summed up in Table 3.

Table 3: Designed modulator parameters

Parameters	Value
Technology	0.35 µm
Order of modulator	1
Sampling Frequency (clock)	10.24 MHz
Signal Band width	80 KHz
Over sample Ratio(OSR)	64
References	±1V
Maximum Input	1 V_{pp}
Supply voltage	±1.5V
Resolution	8-bit
Signal to Noise Ratio (SNR)	49.25 dB
Quantizer resolution	1 bit
Power consumption	5.5 mW

Table 4: Comparison table of most popular designs with current work (*)

Resolution	OSR	SNR (dB)	Speed (MHz)	Power (mW)	Process (CMOS)	Signal Band width	Order	Ref. No.
14-bit	24	85	2.2	200	0.35µm	100 KHz	6	12
11-bit	10	62.5	300	70	0.13µm	15 MHz	4	13
14-bit	96	85	53	15	0.18µm	300 KHz	2	14
16-bit	128	-	5.12	2.6	0.18µm	20 KHz	3	15
8-bit	64	49.7	1.024	6.6	0.6µm	8 KHz	1	16
8-bit *	64	49.25	10.24	5.5	0.35µm	80 KHz	1	This Work

The current state of the art in the design of ΣΔ modulator is limited by the technology and the sampling speeds it is able to achieve. Here is a comparison table 4 of the most popular designs which also compares the published works with the current work. It can be seen that the current work consumes less power than most published work and achieves the resolution of 8 bits using one of the technology 0.35 µm CMOS process.

CONCLUSIONS

The low-power-consumption modulator is designed with switched-capacitor techniques, and the resolution reaches 8 bits in 0.35 µm CMOS process. Compared to other ΣΔ modulators, the first order single ΣΔ modulator has many advantages on performance, stability, area and system specification requirements, especially the power consumption. When the power supply is ±1.5 V, the power consumption is only 5.5 mW.

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