IMPLEMENTATION OF DELAY MEASUREMENT TECHNIQUE USING SIGNATURE REGISTER FOR SMALL-DELAY DEFECT DETECTION

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Abstract

This paper proposes an method for testing a circuit in order to improve defect coverage of delays due to resistive open and close. The proposed method uses a signature analysis and a scan design to detect small delay defects. This measures the delay of the explicitly sensitized paths with the resolution of the on-chip variable clock generator. The proposed scan design measures the small delay in short measurement time by delay measurement technique and extra latches for storing the test vectors. By evaluating with Rohm 0.18-µm process shows that the measurement time is 67.8% reduced compared with that of the delay measurement with standard scan design and the area overhead is larger than that of the delay measurement architecture using standard scan design.

Index Terms: *Very Large Scale Integration (VLSI), Large Scale Integration (LSI), Design for Testability (DFT)*

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1. INTRODUCTION

Modern VLSI chips have stringent timing requirements driven by shrinking feature sizes. This has resulted in the emergence of delay faults as a significant problem and introduced the necessity to detect delay faults. The major types of defects that occur during the manufacturing of ICs are opens and shorts. The electrical impact of these defects strongly depends on their resistance. Low-ohmic shorts and high-ohmic opens in general cause a logic failure and are therefore easy to detect during testing. The detection of 'resistive' shorts and opens is harder. The electrical impact of these defects is smaller and it is missed by a slow conventional stuck-at test. Nevertheless, the detection of resistive opens is a requirement to achieve low defect levels. The resistive open typically introduces an additional delay due to which the IC cannot perform at the intended frequency. To detect these opens one usually uses a transition fault test or a functional test. Transition fault patterns can be created with ATPG with the advantage of a higher fault coverage and a better fault localization than what is typically achievable with functional patterns. Small delay faults are usually masked since their impact is too small compared with the delay of the longest path (which determines the maximum test speed). This is due to the fact that the generated patterns have unequal path lengths and a small delay in a short path can still meet the speed during testing. These small delays can cause a fail if they are activated in a longer path during application. Furthermore, they do form a reliability risk. Therefore development of the embedded delay measurement technique is required. Some embedded delay measurement techniques have been proposed. The scan-based delay measurement technique with the variable clock generator is one of these on-chip delay measurement techniques. In this technique, the delay of a path is measured by continuous sensitization of the path under measurement with the test clock width reduced gradually by the resolution. The main good point of the scan-based delay measurement technique is its high accuracy. The reason of the high accuracy is that the technique measures just the period between the time when a transition is launched to the measured path and the time when the transition is captured by the flip flop connected to the path, directly. The variation of the measured value just depends on the variation of the clock frequency of the clock generator. Therefore, if the clock generator is compensated the influence of the process variation, the measured value does not depend on the process variation.

1.1 Existing Method

The scan-based delay measurement technique with the variable clock generator is one of these on-chip delay measurement technique. In this technique, the delay of a path is measured by continuous sensitization of the path under measurement with the test clock width reduced gradually by the resolution. The main good point of the scan-based delay measurement technique is its high accuracy. The reason of the high accuracy is that the technique measures just the period between the time when a transition is launched to the measured path and the time when the transition is captured by the flip flop connected to the path, directly. The variation of the measured value just depends on the variation of the clock frequency of the clock generator. Therefore, if the clock Generator is compensated the influence of the process variation, the measured value does not depend on the process variation.

However, it has a drawback. The measurement time of the technique depends on the time for the scan operation. These

days, the gap between the functional clock and scan clock frequency increases. Therefore the measurement time becomes too long to make it practical.

The flip flop reduces the required number of scan operations, which makes the measurement time practical. They also proposed the area reduction technique of the self testing scan-FF. However, the area overhead of these methods is still expensive compared with the conventional scan designs.

1.2 Disadvantages of Existing System

- Less reliability
- Impossible to measure the small circuit path delays using an external tester, even if the resolution is high

1.3 Proposed System

This paper presents a scan-based delay measurement technique using signature registers for small-delay defect detection. The proposed method does not require the expected test vector because the test responses are analyzed by the signature registers. The overall area cost is of the order of conventional scan designs for design for test (DFT). The measurement time of the proposed technique is smaller than conventional scan-based delay measurement. The extra signature registers can be reused for testing, diagnosis, and silicon debugging.

Various methods for small-delay defect detection have been proposed. The path delay fault testing with a normal clock width is the most popular and is widely used. In this method, we choose the longer paths to detect the smaller cumulative delay due to the small delay distributed on the paths. The larger the cumulative delays, the higher the probability of the detection of the distributed small delay. However, the coverage of the small delay defect detection largely depends on the normal clock width, which is a problem of this method. On the other hand, to solve the problem, methods with delay fault testing using a variable clock generator have been proposed. The delay fault testing with a smaller test clock reduces the slack of the paths. Therefore the smaller delay defects which cannot be captured with the normal clock width can be captured with the appropriate smaller test clock width.

1.4 Advantages of Proposed System

The proposed method does not require the expected test vector because the test responses are analyzed by the signature registers. The measurement time of the proposed technique is smaller than conventional scan-based delay measurement.

1.5 Variable Clock Generator

In addition, it can be used not only for the detection of small delay defects, but also for the debugging. Because modern chips are too huge and complex, LSI CAD tools cannot optimize the design enough. Hence, the manufactured first silicon chip usually does not meet the specification in spite of the tighter release to production (RTP) schedule. Therefore silicon debugging and design for debugging (DFD) become much more important in modern chips.

Various silicon debugging technologies and DFD methods have been proposed. On-chip delay measurement provides accurate information of the delay of inside paths for the debugging of small-delay defects.

In the proposed method, the clock width should be reduced continuously by a constant interval as explained later this clock operation. Therefore an on chip variable clock generator is indispensable for the proposed method.

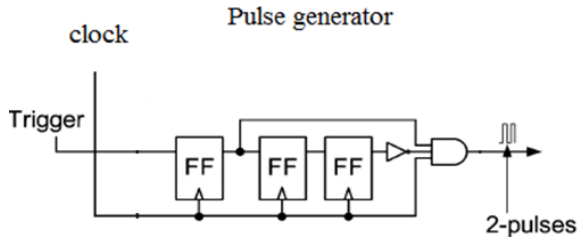

Fig -1: Variable clock generator

2. DELAY MEASUREMENT TECHNIQUE USING SIGNATURE REGISTER

Basically, the proposed method is scan-based delay measurement. The difference from the basic one is the usage of the signature registers and the additional latches for the acceleration of the delay measurement. first, we assume that each flipflop has its own extra latch. The value of each flipflop is stored in the correspondent latch, and the value of each latch can be loaded to the correspondent flipflops in arbitrary timing. In the proposed measurement, the test vector is stored in these latches after scan-in operation. Once the test vector is stored in the latches, the test vector can be loaded from these latches in a clock without scan-in operation. It reduces the time for multiple sensitization of a path drastically.

2.1 Scan Flip Flop for Measurement

Fig. 2 is the gate level description of the scan flipflop for the proposed measurement. The lines D, Q, and clk are the input, output, and clock lines, respectively. The lines si and so are the input and output and clock lines, respectively. The line latch is connected to an extra latch which provides the test bit of flip flop. The lines si and so and are the input and output for constructing the scan path. The input is connected to an adjacent scan flipflop or the scan input. The output is connected to of an adjacent scan flipflop or the scan output. The flipflop has two multiplexers. The lines si and latch are the inputs of the upper multiplexer controlled by se1.The output of the upper multiplexer and D are the inputs of the bottom multiplexer controlled by se0. When se0=1 and se1=1,

the flip flop is in scan operation mode. When se0=1, se1=0, the flip flop loads the value stored in the latch connected to the latch line.

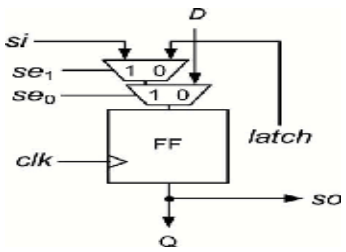

Fig -2: Scan flip flop

2.2 Reconfigurable Signature Register

The signature register for the proposed measurement requires the following functions to meet the demand of the proposed measurement.

- Capturing the test response in arbitrary timing.
- Shifting out the signature data in arbitrary timing.

Figure. 3 shows the architecture of the signature register for the proposed measurement. The length of the signature register in this example is four bit. Therefore it has four flipflop FF0, FF1, FF2, FF3. The signature register can be configured to a shift register. The line sge controls the configuration. When sge=1, it works as a signature register. When sge=0, it works as a shift register. The line in is the input of the signature register. During measurement, test responses are sent to in. The line clk is clock line. The clock line is controlled by sck. When sck=0, the signature register does not capture the input value. When sck=1, the signature register captures the input value synchronizing with the positive edge of clk. By controlling sck, the signature registers capture only the target test response.

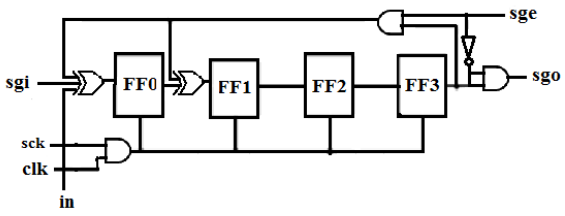

Fig -3: Reconfigurable Signature Register

When sge=0, this circuit is configure to the shift register. The input is sgi. The output is sgo. The measurement system requires multiple signature registers generally. The input and output are connected to the output and the input of adjacent signature registers to construct a long shift register for sending all the signature values to the external tester.

3. DELAY MEASUREMENT SYSTEM

Figure. 4 shows the proposed measurement system. The proposed system consists of the low cost tester and the chip with the variable clock generator (VCG) and a BCD decoder. The chip is assumed to have single functional clock in the proposed method, and the chip has two reset lines for initializing the flipflop and the signature registers independently. The low cost tester controls the whole measurement sequence. The clock frequency tck is slower than the functional clock. The line retrieves the signature data from the signature registers to estimate the measured delay. The line sci sends the test vectors to the scan input of the chip. The line sco gets the data of the flipflop from the scan output of the chip. In the proposed measurement sequence, sco is not used. However, it is used to check the flipflop or the additional latch es before the measurement. The line cs is the clock control line.

The proposed measurement uses both the slow tester clock tck and the fast double pulse generated by on-chip VCG. The line cs selects the slow and fast clock. If cs is 1, the fast clock is sent to the clk clock line of the components. Otherwise the slow tester clock tck is sent. The lines trg and cnt are the input lines for VCG. The fast double pulse is launched synchronizing with the positive edge of clk. The line scj0……..scjl-1 controls the width of the double pulse. The line controls the scan flip flops. The line controls the latches for storing test vectors. The lines are the inputs for the encoded data to control the capture operation of the signature registers. The BCD decoder decodes the encoded input data to the control data of the signature registers, the decoder is used to reduce the input lines for the control data of the signature registers. The sge is the enable signal for the signature registers. The flip flops in the chip are classified to the clusters clo……..cl(m-1).

3.1 Measurement Sequence per a Test Vector

When the measurement system has m signature SIGo…SIG (m-1), m paths can be measured in parallel maximally. To reduce the measurement time we measure multiple paths simultaneously.

We explain the measurement strategy using the example depicted in Fig. 5. In this example, the proposed method is applied to the circuit with six flip flops FFo- FF5. These flip flops are classified to the two clusters Clo and Cl1. the cluster Clo includes (FFo, FF1, FF2), and Cl1 includes FF3, FF4, FF5. The cluster Clo has the signature register SIGo. The cluster Cl1 has the signature register SIG1. The paths p1,p2,p3,p5 are sensitized simultaneously by the test vector (FFo,FF1,FF2, FF3,FF4,FF5) = (0,0,1,0,1,1).

The test response pi of is captured by FFi. The expected test response is (FFo,FF1,FF2, F3,FF4,FF5)=(1,1,0,1,0,0).The paths p1 and p2 are measured by SIG0. The paths P3 and P5

are measured by SIG1. The combination of the two paths, one of which is selected from P1 and P2, the other of which is selected from P3 and P5, can be measured simultaneously.

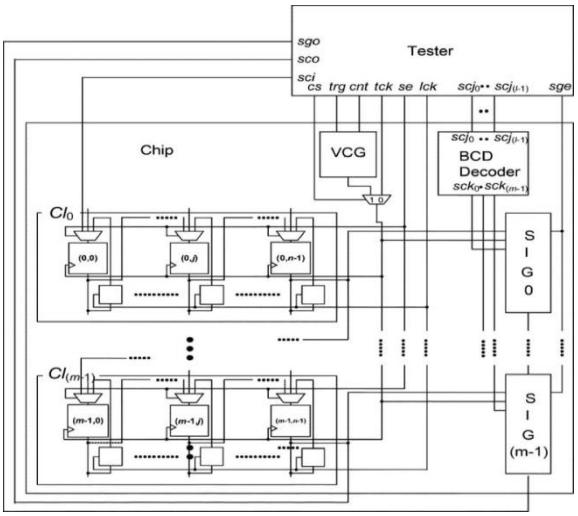

Fig -4: Delay Measurement System

Although the four paths are sensitized by the test vector, two paths can be measured simultaneously at most. Hence, we measure the four paths divided into two measurement stages STG0 AND STG1 each of which measures two paths P1 and P5 in STG0 and P2 and P3 in STG1 simultaneously. First, the test vector is set to the flip flops with scan-in operation. After that, the values of the flip flops are set to the extra latches (a). Second, the first stage measurement is performed (b). Third, the second stage measurement is performed (c).

In each stage, the paths under measurement are tested multiple times with reducing the test clock width. Steps (b) and (c) show the state just after the test execution. The flip flops hold the test response. The latches hold the test vector. After the testing, the test responses are shifted to the signature registers SIG0 and SIG1 and with the clock operation of clk . The required number of shift clocks of a stage is the maximum number of the shift clocks among the paths measured simultaneously in the stage. For example, in STG0, two clocks are required to send the test response of P1 to STG1, while one clock is required to send the test response of P5 to SIG1.
To capture only the target test response value, the control bit sequences are sent to sck0 and sck1. In SIG0, the test response of P1 is captured to FF1. Therefore SIG0 should capture the value two clocks later. This operation is realized by sending the bit sequence "01" to sck0 synchronizing to clk . To capture the test result of p5, SIG1 should capture the value one clock later. This operation is realized by sending the bit sequence "10" to synchronizing sck1to the clk in STG0. In STG1, the test response of P2 is captured by sending the bit sequence "100" to sck0, and the test response of P3 is captured by sending the bit sequence "001" to sck1, respectively.

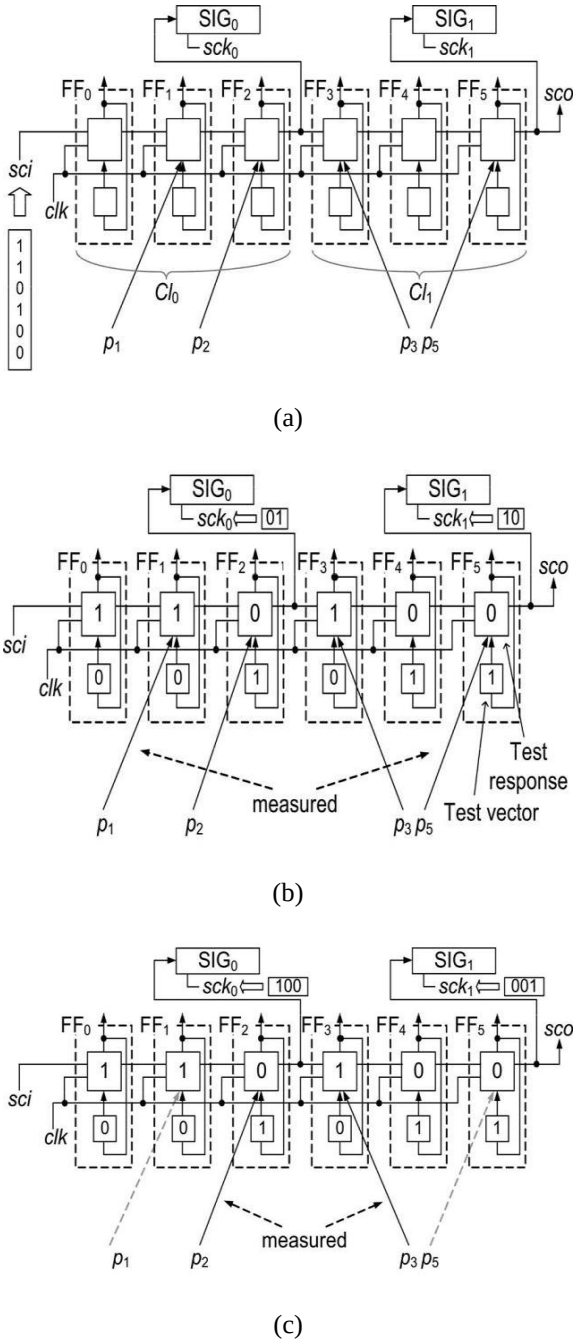

Fig -5: Measurement of Paths Sensitized in a Test Vector in Parallel.

Fi-6 shows the timing chart of this operation. The low cost tester controls the whole measurement sequence. For the measurement both VCG clock and tester clock are used. The clock selection is controlled by cs. The trigger signal trg and the control signal cnt is provided to VCG. The control data cnt is updated after each testing operation. In STGo, STG1 captures the test response in the second shift-out clock. Therefore sck0 turns to 1 synchronizing with the negative edge of the first clock of the shift-out operation.The latch

clock lck captures the values of the flip flops just after the scan-in operation is finished. The se0, se1, se2 are controlled as explained previously

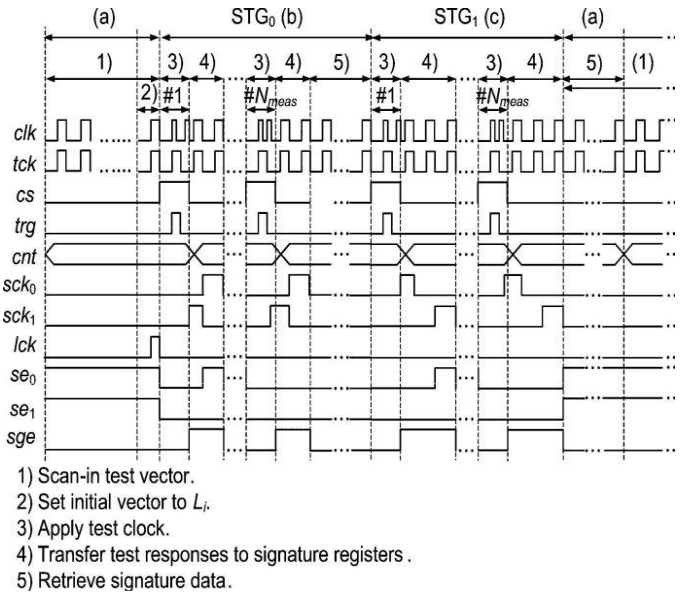

Fig -6: Timing Chart of the Sequence of Fig-5

3.2 Whole Measurement Sequence

Here, we assume that the test set for the measurement TS has N TV test vectors tv0, tv1,...tvNTV-1. The number of the stages of tvi is Nst (i) . Before measurement, we have to check if the flip flops, the latches, and the clock generator work correctly by applying test vectors or other checking methods. After that, the following measurement sequence is executed.

Step 1: Initialize the variable i=0.
Step 2: If I is equal to Ntv, finish, otherwise initialize the variable j to 0, and set tvi to the flipflop with scan-in operation.
Step 3: Send the values of the flipflop to the latches.
Step 4: The paths included in STGj are measured Simultaneously. After that is updated to (j+1).
Step 5: If j is equal to Nst (i, go to Step 6, otherwise load the test vector from the latches to flip flops, and go to Step 4.
Step 6: I is updated to (i+1) , and go to Step 2.

3.3 Tester Channel Reduction

If sck of each signature register is directly fed to the input of the chip, it requires the same number of the extra inputs as the of the signature registers. It increases tester channel width. To keep the tester channel width short, we use the BCD decoder as depicted in Fig. 6. The decoder circuit transforms n bit binary code to the corresponding 2^n width decimal code. For example, when n=2, scj0scj1=01,the corresponding decimal code is sck0sck1sck2sck3=0100.

We explain how to encode the sck bit sequences to the corresponding binary code scj with the example depicted in fig 9.This example consists of three clusters cl0, cl1,and cl2. Each cluster has three flip flops. Consider the case that the test response of the sensitized flip.paths captured in FF01, FF12, and FF20.In the shift out operation after a testing, the test response of FF01 is captured by SIG0 two clocks later. Therefore the bit sequence “010” should be sent to sck0.the test response of FF12 is captured by SIG1 one clock later.

Therefore the bit sequence “100” should be sent to sck1.The test response of FF20 is captured by SIG2 three clock later. Therefore the bit sequence “001” should be sent to sck2.each bit value of these bit sequences is grouped. the group of the 0th bit values is sck0sck1sck2=010.those of the first bit values and second bit values are sck0sck1sck2=100, sck0sck1sck2=001,respectively. We call each group slice. Here, sli represents the slice of the ith bit .Finally, these decimal codes are transformed into the corresponding binary code .The 0th slice sl0 “010”is transferred to”01” The 1st slice sl1 “100”is transferred to”10” the 2nd slice sl2 “001”is transferred to”11”.

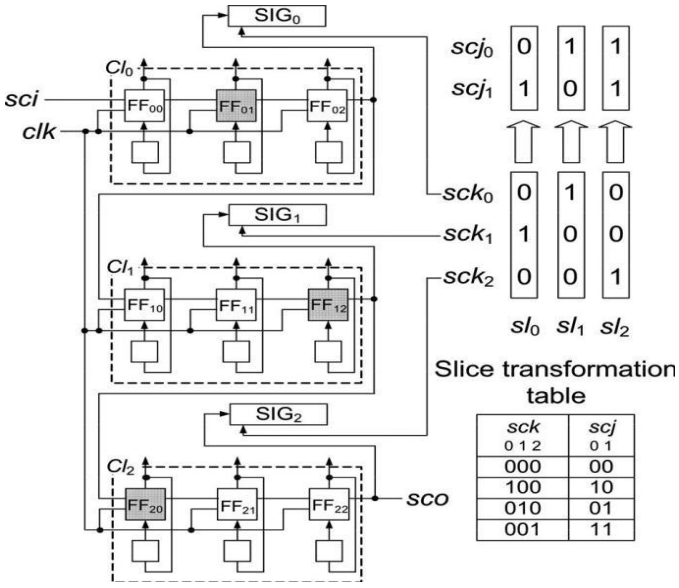

Fig -7 Encoding the Output Data of BCD Decoder to the Input Data of BCD Decoder

As a result, the bit width of the data is reduced from 3 bit to 2 bit by this transformation. Generally, the width of the slice of sck is n, the width of encoded slice of scj is [log2n] .However, for the encoding, each slice is permitted only 1 bit with the value 1. More than two bits with value 1 is not permitted. This restriction puts the constrain on ATPG for the generation of the test set for the measurement.

4. EXPERIMENTAL RESULTS

In this section, on-chip path delay under different process variations will be simulated and measured. During the simulation we measure the delay of each path under test. Random faults were injected in circuits to generate erroneous data. Random input patterns were applied to the ISCAS-89 benchmark circuits and compared with proposed method. The length of the signature register is 8 bit. The test set consists of test vectors which detects all single-path sensitizable transition faults. The paths sensitized by these test vectors are measured. The measurement time using the proposed scan design and is calculated by

Tsig=time required for {whole scan-in + double pulse + SIG data}

Table –I: Measurement time

Circuit	EMB	T_{sig}	R_t
S5378	635.4	181.2	71.5
S9234	703.1	135.5	80.7
S38584	4025	1011.5	72.6
Ave			74

Table -II: Comparison With Delay Measurement Using Embedded Delay Measurement Circuit

Circuit	EMB	SIG	R
S5378	46.7	181.2	3.9
S9234	164.5	135.5	0.8
Ave			2.3

The proposed method is compared with the delay measurement with conventional scan design, namely standard scan design and enhanced scan design. The length of the cluster size is restricted to 32. The measurement time is shown in Table I and this method is compares with delay measurement using embedded delay measurement circuit shown in Table II. The Device utilization summary for the delay measurement technique is shown in Table III.

Table –III: Device Utilization Summary

Logic Utilization	**Used**	**Available**	**Utilization**
Total number of slice register	43	7168	1%
Number Used as Flip Flops	31		
Number Used as Latches	12		
Number of 4 input LUTs	47	7168	1%
Number of occupied Slices	47	3584	1%
Number of Slices containing only related logic	47	47	100%
Number of Slices containing only unrelated logic	0	47	0%
Total Number of $ input LUTs	47	7168	1%
Number of bonded IOBs	13	141	9%
Number of BUFGMUXs	3	8	37%
Average Fanout of Non-Clock Nets	2.76		

CONCLUSIONS

We have presented a measurement technique, based on signature analysis, for screening small-delay defects and we also generated an on-chip variable clock generator for double pulse width and latches for short measurement time in scan design and compared with standard scan design. A future work is extension of cluster and implementation of FPGA with low cost application.

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