LOW POWER SRAM DESIGN USING BLOCK PARTITIONING

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Abstract

Technology scaling results in significant increase of leakage currents in MOS devices due to which power consumption in Nano scale devices increases. As memory accounts for the largest share of power consumption, thus there is need to design such a memory which will consume less power.

Through this paper, we propose a systematic approach by Block partitioning which provides a methodology for reducing the dynamic power consumption of SRAM (static random access memory). Dynamic power dissipation in memory is due to charging/discharging of long capacitive lines (bit line and world line). So by block partitioning our goal is to reduce length of world line as well as bit line capacitances. instead of implementing 1KB SRAM at a time we are designing four blocks of 256 byte RAM, which reduces world line from 1024 bits to 256 bits. We implemented our design on TANNER TOOL using 180 nm technology

Keywords-*Low power, SRAM, 6T cell, Dynamic power.*

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1. INTRODUCTION

Low power SRAM (static random access memory) has become a critical component of many VLSI chips. Power dissipation has become an important consideration both due the increased integration and operating speeds as well as due to the explosive growth of battery operated appliances. When working with RAM we encounter two problems. First, increasing size of memory increases length of high capacitive lines (bit line and world line). This in turn Increases power consumption and delay. With the help of partitioning of SRAM we activate only desired bit line for read and write operation [1]. Two types of power dissipation in nano-scale MOS- devices are dynamic power dissipation and Static power dissipation. The sum of the power consumption in decoders, bit lines, data lines, sense amplifier, and periphery circuits represent the active power consumption dissipated in bit lines represents about 60% of the total dynamic power consumption during a write operation [2,3,4]. Designing a low power system not only Reduces weight and size of batteries for portable systems but also helps in reducing the ever-important packaging costs of integrated circuits

2. BLOCK DIAGRAM OF SRAM

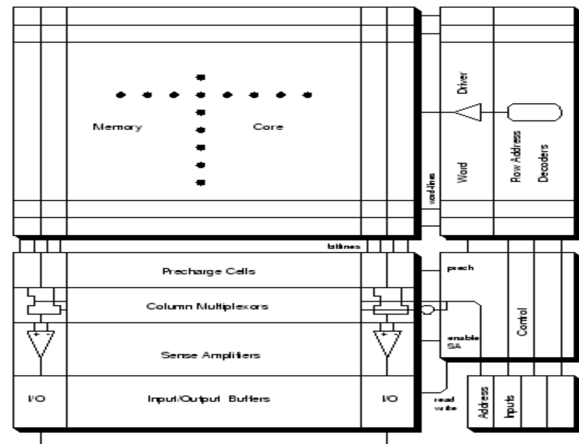

Fig.1 Block diagram of SRAM

2. MEMORY ADDERSSING

We accessed the memory through different peripheral circuitry.

2.1 Row Decoder

A row decoder is used to decode the given input address and select the word line. When performing a write or, read operation only one of the row is selected and 8 bits of data is transmitted schematic of 8x256. Decoder is shown in fig .2.

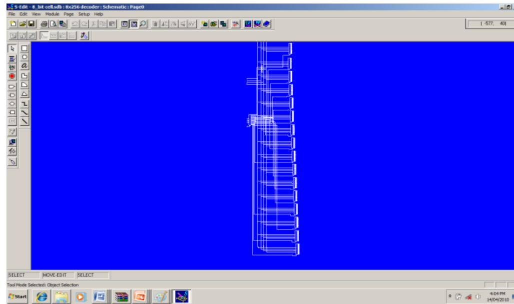

Fig.2-schematic of 8x256 row Decoder

In our design we have 256 rows and each row contains 8 cells. The row decoder selects one of those rows, depending on the 8 bit address given to it. In order to design a one bank of 256 byte SRAM a 8x256 decoder is used. Number of word line equals to the number of rows in the SRAM cell array. In our design a NAND based decoder is used. NAND based design is suitable as it faster.

2.2. Column decoder (mux)

For designing 1KB SRAMs we designed four blocks of 256 bytes. Output of 8:256 decoder is common to all four banks .Schematic of 4x1 mux is shown in fig.3

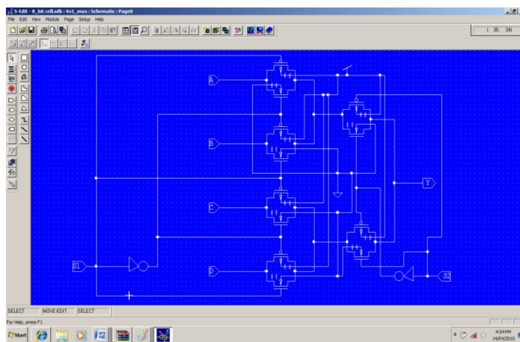

Fig.3-Schematic of 4x1 mux

So to select only one bank at a time we use eight single bit 4x1 mux.

2.3 Sense amplifier

A sense amplifier circuit is used to read the data from the cell. In addition, it helps reduce the delay times and minimizes power consumption in the overall SRAM chip by sensing a small difference in voltage on the bit lines. Schematic of sense amplifier is shown in fig.4

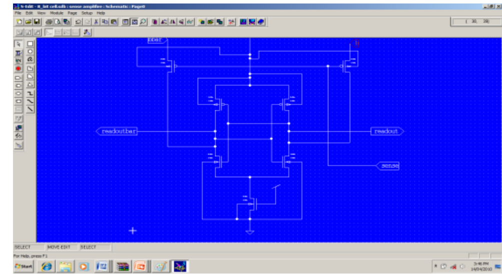

Fig .4-schematic of sense amplifier

A low-voltage sense amplifier is used in our SRAM design to support high performance. 8 sense amplifier circuits were used for the SRAM design, one for each column. For designing the sense amplifiers cross-coupled inverters are used to sense a small change of the voltages on the bit-line and the bit-line bar. The sense amplifiers are only active during the read operation. During the read operation the resulting signal gives a much lower voltage swing, to compensate for the swing a sense amplifier is used to amplify voltage coming off the two bit lines, bit-line and bit-line bar.

2.4 Control signal:

We have included three control signals wr_en (write enable), rd_en (read enable), EN(enable) in our design to perform proper read/write operation .

2.4.1 Pre-charge Circuit

The function of the pre-charge circuit is to charge the bit-line and inverse bit-lines (bit-line bar) to 5 V. The pre-charge enables the bit-lines to be charged high at read cycle.

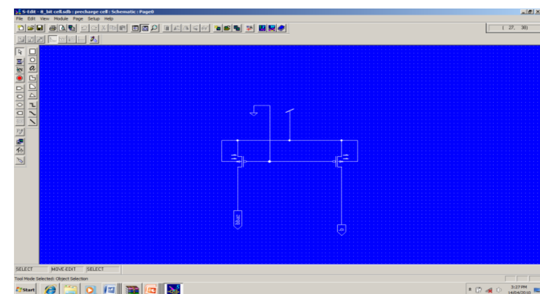

Fig.5-schematic of pre-charge circuit

Figure 5 shows the schematic of the pre-charge circuit. The PMOS transistors used for the pre-charge circuit are 1.5 µm each, the smallest width transistors.

3. SRAM CELL

In our design we have chosen full CMOS 6-transistor cell for the cell array.

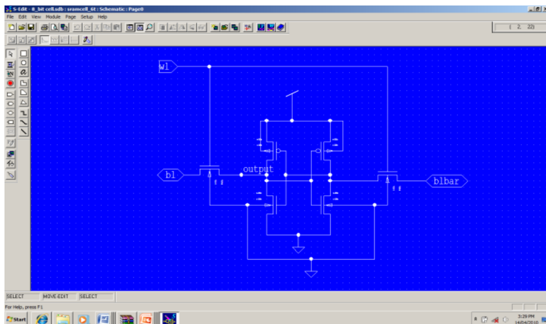

Fig.6-schematic of six transistor SRAM cell

Figure 6 shows the schematic of the 6-T cell. The 6-T cell consists of two cross coupled inverters connected with the two NMOS transistors on both the ends. Each NMOS transistor is connected to an inverter on one side and bit line on the other side. The data value is stored in the net connected to the left side of the NMOS in figure 6. The inverse data value is stored in the net connected to the right side of the NMOS in figure 6. The input signal A0 in the figure 3 comes from the row decoder, allows the cell to be connected to the complementary bit lines during reading and writing and disconnects otherwise. To determine the sizes of the transistors of the cell, simple W/L ratios shown in equation 1 and equation 2 were used.

$$\frac{K_{n,3}}{K_{n,1}} = \frac{(W/L)_3}{(W/L)_1} < \frac{2(V_{DD} - 1.5V_{T,n})V_{T,n}}{(V_{DD} - 2V_{T,n})^2} \qquad (1)$$

$$\frac{K_{p,5}}{K_{n,3}} = \frac{(W/L)_5}{(W/L)_3} < \frac{\mu_n}{\mu_p} \frac{2(V_{DD} - 1.5V_{T,n})V_{T,n}}{(V_{DD} + V_{T,p})^2} \qquad (2)$$

In the equations the subscripts show the transistor number from figure 6. Equation 1 shows a simple relation between two nmosN3 and N1[5,6]. Equation 2 shows a simple relation between PMOS P5 and NMOS N3.Using the two equations, approximate values of the widths of the transistor were calculated and the design was simulated. The final wn and wp values are shown in figure

4. POWER REDUCTION CONCEPT:

If suppose Power consumption of one bank (256_bytes) =P .Then total power of four bank (256x4=1k) =4P (Theoretically) Let power consumption after partitioning (1k_byte) =x, then for desired result x<4P

5. SRAM POWER REDUCTION BY BLOCK PARTITIONING

As described active power is major component of total memory power .This paper develops systematic approach for implementing 1kB SRAM using block partitioning shown in fig.7 [7, 8]. As seen in figure.7 each bank is of 256 Bytes. Output of 8x256 decoder is common signal to all four banks.

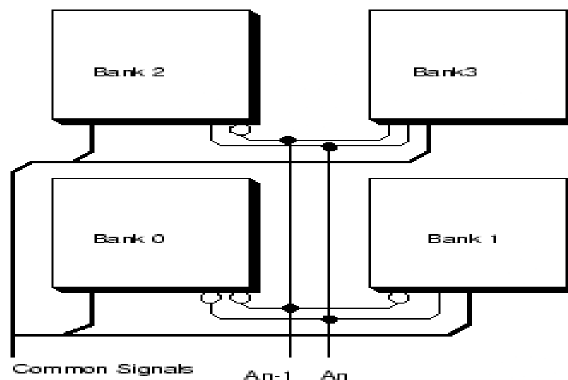

Fig7.-SRAM block partitioning

Select signal		Selected bank
An	An-1	
0	0	Bank 0
0	1	Bank 1
1	0	Bank 2
1	1	Bank 3

An-1 and An are select signals of 4x1 mux. According to select line given in above table, mux will select only one corresponding Bank at a time. Thus instead of using 1024 world line we are using 256 world lines only. Thus block partitioning targets total switching capacitance to achieve reduced power and improved speed. It will also reduce dynamic power and Column read current.

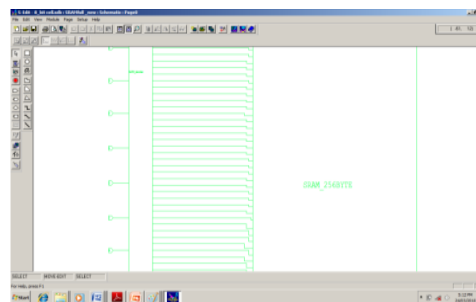

Fig.8 Schematic of one Bank (256_Byte) SRAM for read /write operation

6. RESULT AND CONCLUSION

Average power is calculated for the design by carrying out transient analysis and is found to be as following:

1KB un-partitioned SRAM: 1.243 uW.
1KB partitioned SRAM: 0.8712 uW

Hence it is concluded that block partitioning reduces the dynamic power consumption of SRAM.

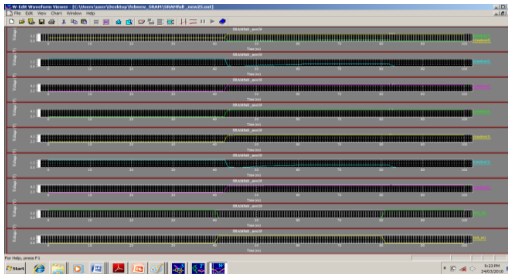

Figure 9: Transient analysis of SRAM

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