

# LOW POWER SRAM USING ATD CIRCUIT

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## Abstract

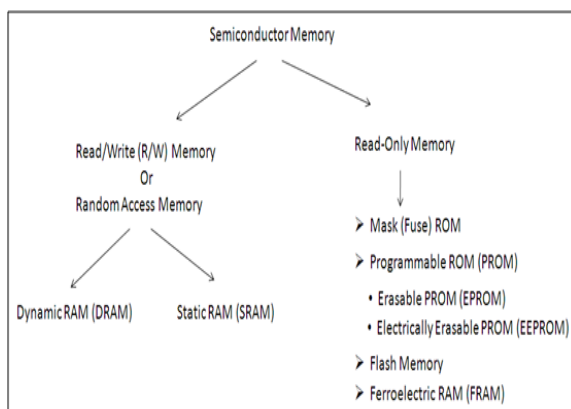
The address signal lines are connected to a semiconductor memory device when they are implemented on the PCB (Printed Circuit Board). So they experience the wiring capacitance and due to this wiring capacitance on printed circuit board the rising and falling time of respective address signal disperse. If the address signal lines change in timing, the following problem occurs. When a microprocessor connected to a semiconductor memory device changes the address information from one address to another address, due to deviation of timing of the change of the signal, the wrong address is generated. In an Asynchronous semiconductor memory device, the change of address is immediately responded. So it also responds to such wrong address information and internal circuit selects the wrong address information and operates corresponds to that wrong address.

**Key words:-** OFDM, STBC, SWITCHING, PATH FADING.

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## 1. INTRODUCTION

Based on the operation type of individual data storage cells, RAMs are classified into two main categories. Dynamic RAMs (DRAM) and Static RAMs (SRAM). The DRAM cell consists of a capacitor to store binary information, 1 or 0, and a transistor to access the capacitor. Cell information is degraded mostly due to a junction leakage current at the storage node. Therefore, the cell data must be read and rewritten periodically (refresh operation) even when memory arrays are not accessed. On the other hand, the SRAM cell consists of a latch, therefore, the cell data is kept as long as the power is turned on and refresh operation is not required. The classification of memories is as shown in following chart.



**Figure 1.1:** Classification of Memory

Read-only Memory (ROM) allows, as the name implies, only retrieval of previously stored data and does not permit modifications of the stored information contents during normal operation. ROMs are nonvolatile memories. Depending on the

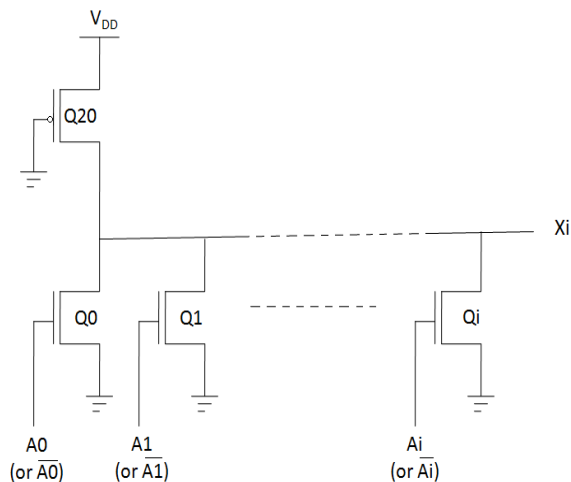
type of data storage (data write) method, ROMs are categorized as Mask ROM, in which data are written during chip fabrication by using a photo mask, and Programmable ROM (PROM), in which data are written electrically after the chip is fabricated. Depending on data erasing characteristics, PROMs are further classified into Fuse ROM, Erasable PROM (EPROM) and Electrically Erasable PROM (EEPROM). The data written by blowing the fuse electrically cannot be erased and modified in Fuse ROM. DATA in EPROMs and EEPROMs can be rewritten, but the number of subsequent re-write operations is limited to. Flash memory is similar to EEPROM, where data in the block can be erased by using a high electrical voltage. A drawback of EEPROM is the slower write speed, in the order of microseconds. Read write (RW) memory must permit the modification (writing) of data bits stored in the memory array, as well as retrieval (reading) on demand. The read write memory is commonly called Random Access Memory (RAM), mostly due to historical reasons. Unlike sequential-access memories such as magnetic tapes, any cell can be accessed with nearly equal access time. The stored data is volatile; i.e., the stored data is lost when the power supply voltage is turned off. A system based on this approach consists of one or more subsystems which are surrounded by an environment with which they communicate. The information and state of the system is usually held in storage elements and is allowed to flow between those during the duration of a discrete time interval. In synchronous design the boundaries of this time interval are physically represented by the rising and falling edges of a clock signal generated by a global clock generator. These edges are used to trigger the storage elements to store the new information on their inputs. Since the information must be stable before storing it, the length of the time interval is determined by the worst case performance of the slowest operation of the system. Unfortunately this forces operation that is faster and thus completes early to idly wait for

the next occurring clock edge. The storage elements are often represented by registers in the form of flip-flops or transparent latches. Designing a test memory core an its peripherals: The task is to be executed by designing an asynchronous SRAM core (4 \* 4) row and column decoders and current amplifier. Designing an ATD circuit for above said memory core. Testing the ATD circuit for functional verification with the SRAM memory core.

**2. ASYNCHRONOUS RAM AND ADDRESS TRANSITION DETECTOR**

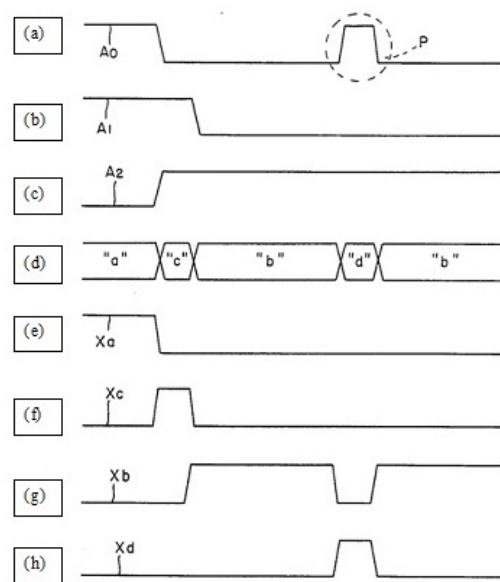
**DETECTOR**

Such an asynchronous semiconductor memory device immediately follows change of the address signals A0-Am and performs the decoding operation at the row decoder RD and the column decoder CD. A single word line (not shown) in the memory cell array is selected by the row selection signal X and a single data on plurality of bit lines (not shown) is selected by the column selection signal Y, and thereby such data is output through the I/O gate and data output buffer DB0 . The row decoder RD of a number of Fig. 2.3 is composed of the decoder circuit



**Figure 2.1:** Schematic Diagram of Conventional Decoder Circuit

such as shown in Fig. 2.1, the number being equal to the number of row selection signals X0 - Xk, and each decoder circuit outputs selection signal when the respective combination of the specified address signals is input.



**Figure 2.2:** Timing Diagram For Conventional Asynchronous Semiconductor Memory

In Fig. 2.1, Q20 is a depletion type MOS transistor, Q0-Qi are enhancement type MOS transistors. When all of the input address signals become low level, the row selection signal X becomes high level. In addition, the column decoder CD is also configured in the same way unwanted power consumption as mentioned above is generated particularly in the input stages of the row and, column decoders as is explained with reference to Fig. 2.2. For convenience of explanation, it is supposed that the 3-bit address signals A0-A2 are input. Fig. 2.2 indicate the address signals A0-A2 and address data "a"- "d" composed of combination of A0-A2 and outputs Xa - Xd of the decoder circuit corresponding to address data "a"- "d". In a process wherein an external device connected to a memory device changes address data from address "a" to address "b", for example, the address signal A1 changes, and in its transitional condition, the address "c" is generated in unwanted form and it is then decoded. When an address changes in such unwanted form, a certain decoder circuit operates as shown in Fig. 2.2e. And a certain decoder circuit operates as shown in Fig 2.2g. But another decoder circuit operates in unwanted way as shown in a Fig.2.2f and it is unnecessary to provide such output. Accordingly, unwanted AC power consumption occurs in the memory device, increasing total power consumption. Such power consumption is also generated in the case wherein a noise signal as indicated by P in Fig. 2.2a is added to the address signal line, even when an external device does not change address data. In this case, the unwanted address "d" as shown in Fig. 2.2d is generated; an output Xb of the decoder circuit which is not required to change may change as shown in Fig. 2.2g, and an output Xd of the decoder circuit which has decoded the address "d" also changes as shown in Fig. 2.2h. Thus unwanted power consumption occurs. When an output of the decoder circuit changes, the circuit connected to the

succeeding stage thereof operated following such change and unwanted power consumption also occurs as explained above. This is the major problem which occurs when dealing with the asynchronous semiconductor memory

### 3. ATD CIRCUIT

In the case wherein a semiconductor memory device is mounted on a printed circuit board, the rising time and falling time of respective signals on a plurality of address signal lines connected to a semiconductor memory device disperse due to the dispersion of wiring capacitance on a printed circuit board. If signals on a plurality of address signal lines change with some scattered deviation in the timing, the following problem occurs.

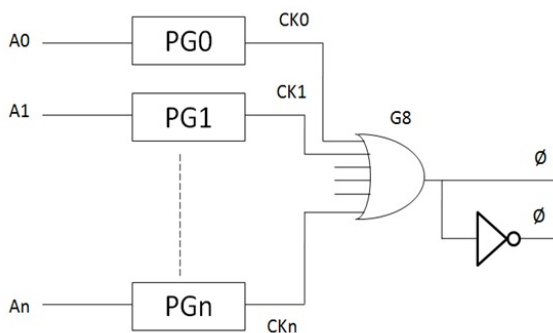


Figure 3.1: ATD CIRCUIT

To avoid above said problem, the change in address signal is detected and hold the internal circuit to a non-operative condition in response to any change of address signal for a specified period. And this is accomplished by the extra circuitry which is called ATD (Address Transition Detection) circuit which generates the pulse of a specified period when one of the address signal changes. This circuit relates to an asynchronous semiconductor memory device and more specifically to a semiconductor memory device which has reduced power consumption as a result of holding an internal circuit to a non-operative condition in response to any change of address signal for a specified period following the change of said address signal

### 4. CIRCUIT LEVEL DESIGN AND FUNCTIONAL VERIFICATION

Figure 4.1 and 4.2 shows the basic block diagram for the interfacing of memory peripherals and memory core with ATD circuit and without ATD circuit which is used for functional verification of the ATD circuit.

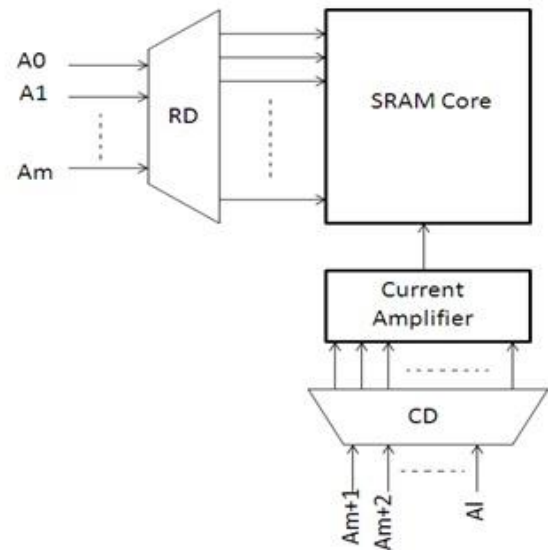


Figure 4.1: Interfacing Of Memory Peripherals and Memory Core without ATD Circuit

Each and every block shown in the Figure 4.1 and 4.2 is implemented in the cadence tool using UMC 180 library used for 180 nm technology and the value of the supply voltage VDD for 180 nm technology is 1.8 volt.

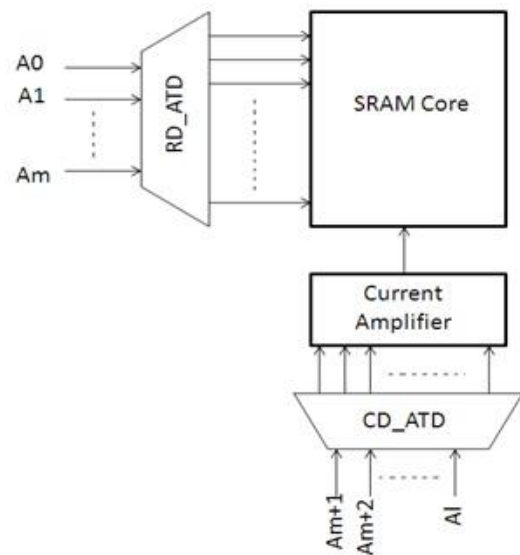


Figure 4.2: Interfacing Of Memory Peripherals and Memory Core with ATD Circuit

#### 4.1 IMPLEMENTATION OF ATD CIRCUIT

For the design of ATD circuit is first of all it is required to design the delay circuit. And here in place of delay circuit a single buffer or the chain of buffer is used. And for that inverter design is require which explain as below.

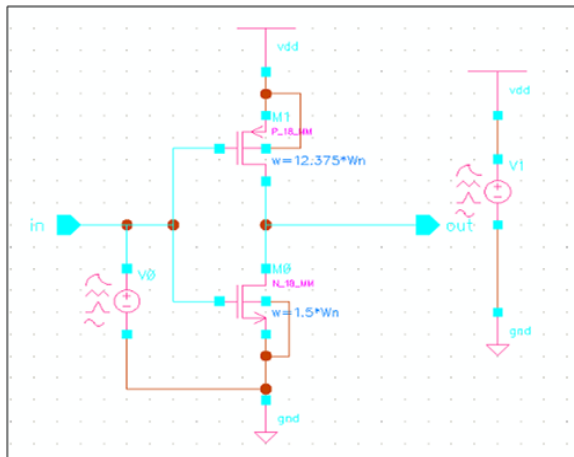


Figure 4.1.1: Schematic of The Circuit For Inverter

To achieve switching threshold  $V_m = V_{DD}/2 = 0.9$  volt and also to reduce the glitch at the transition of the input, the size of the pMOS  $(W/L)_p = 12.375$  and for nMOS it is  $(W/L)_n = 1.5$ .

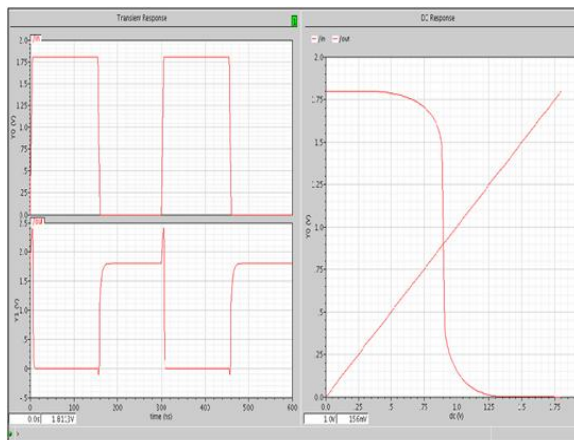


Figure 4.1.2: Transient And DC Analysis For Inverter

Here, from the transient response of the inverter shown in Figure 3.12, it is observed that the switching threshold  $V_m$  is achieved to  $V_{DD}/2$  that is 0.9 volt by keeping the size of transistors as mention earlier. The critical voltage  $V_{IL}$ ,  $V_{IH}$ ,  $V_{OL}$  and  $V_{OH}$  is as given below,  $V_{IL} = 0.795$  volt,  $V_{IH} = 1.032$  volt  $V_{OL} = 0$  volt and  $V_{OH} = 1.8$  volt. From these values the noise margins  $NML$  and  $NMH$  can be calculated.

$$NML = V_{IL} - V_{OL} = 0.795 - 0 = 0.795 \text{ volt}$$

$$\text{And } NMH = V_{OH} - V_{IH} = 1.8 - 1.032 = 0.768 \text{ volt}$$

The rising delay ( $t_r$ ) and falling delay ( $t_f$ ) and also  $t_{pLH}$  and  $t_{pHL}$  of inverter for the unloaded and loaded condition is discuss along with buffer.

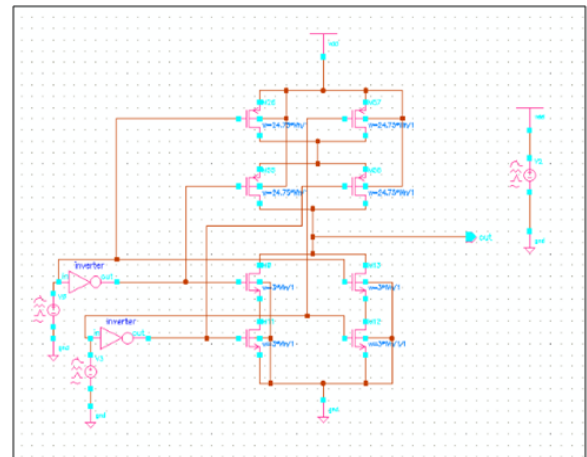


Figure 4.1.3: Schematic Of The Circuit For XOR Gate

Figure 4.1.3 shows the schematic of XOR gate using CMOS in which the size of all the transistors used is decided from the minimum sized inverter that designed earlier. The size of each pMOS  $(W=L)_p$  used in XOR gate is 24.75 and for nMOS it is 3. In the XOR schematic of Figure 3.20, the value of  $W_n$  is 180 nm and length of each transistor is also  $W_n$ . So  $W/L$  ratio of each transistor is same as the multiplication factor with the  $W_n$  which is indicated besides each transistor.

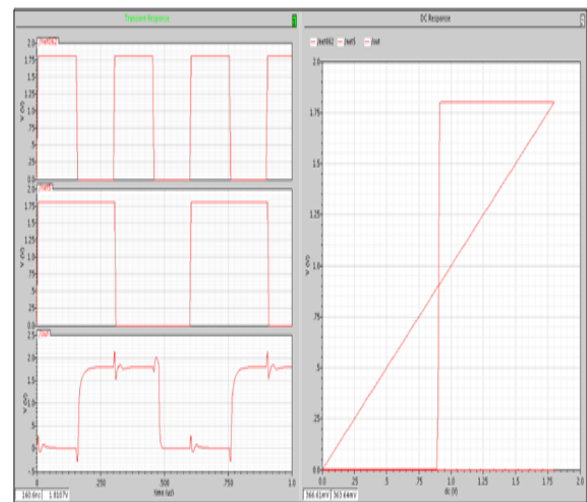


Figure 4.1.4: Transient And DC Analysis For XOR Gate

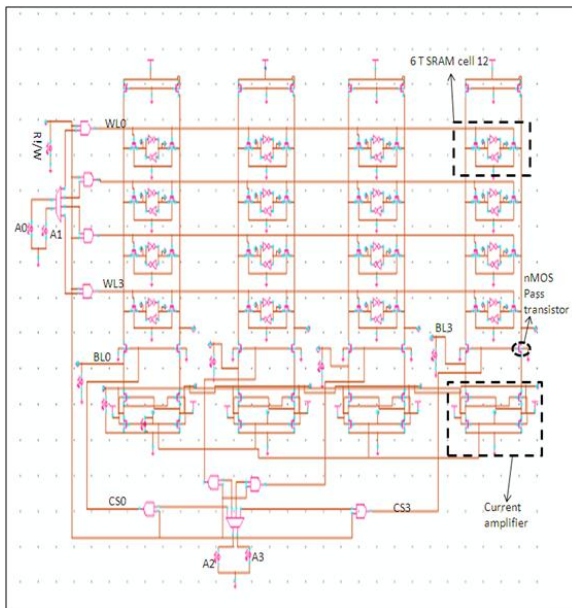
Figure 4.1.4 shows the transient response and the DC analysis of the XOR gate. The transient response shows the two different inputs of the XOR gate with 3.33 MHz and 1.66 MHz of frequencies and the output of the XOR gate which is high only when both the inputs are unequal (01 and 10) and the DC analysis shows the switching threshold of the XOR gate which is 0.9 volt.  $t_{pLH}$ ,  $t_{pHL}$  and  $p$  for the output of XOR circuit for different loaded condition is mention in table 4.1 below.

**Table 4.1:** Transient Analysis For XOR Gate

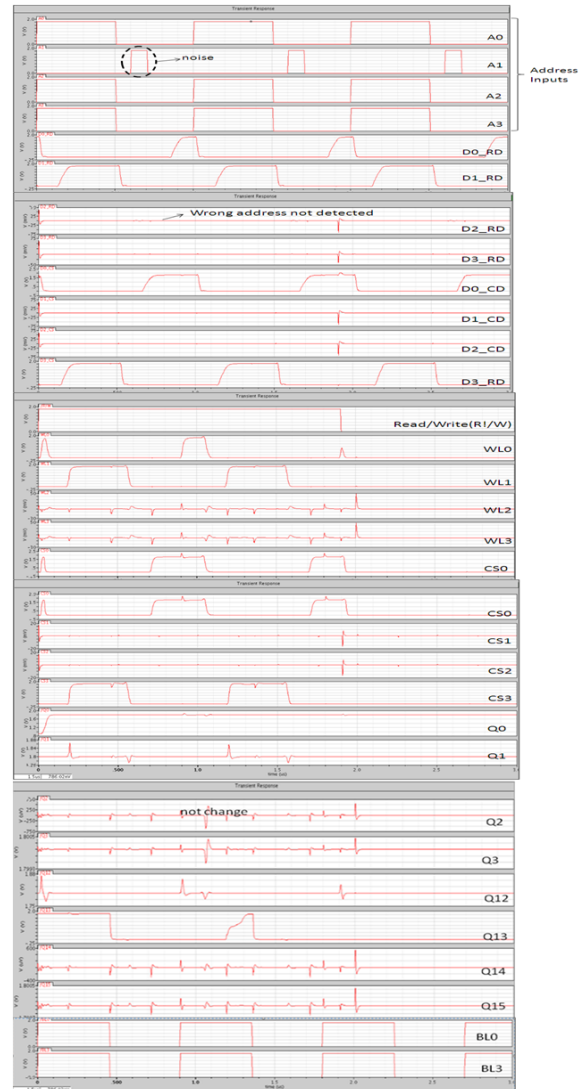
	Load (fF)	$t_{PLH}$ (ns)	$t_{PHL}$ (ns)	$\tau_p$ (ns)
1.	No Load	10.25	21.54	15.89
2.	5	10.81	22.10	16.45
3.	75	16.59	28.90	22.74
4.	100	18.34	31.12	24.73
5.	150	21.56	35.23	28.39
6.	200	24.47	39.08	31.775

**4.2 SIMULATION RESULTS**

Figure 4.1 shows the SRAM array which has 4 \*4 (16) SRAM cells with row and column decoder which are without ATD circuit. According to the status of the address lines and R!/W, reading or writing operation can be performed. Writing operation is done through BL. According to address line status the corresponding output of decoder goes high. And word line status depends on the R!/W which select the complete row of the cell and for particular selection of cell the output of decoder goes high depends on inputs address of column decoder. So the reading or writing operation can be performed to that particular cell. Written or readied data can be seen through Q.



**Figure 4.1:** Schematic of the Circuit For 16 Cells With Row And Column Decoder



**Figure 4.2:** Transient Response for SRAM With ATD Circuit

Figure 4.2 shows the transient response of the reading and writing operation to the cell with introducing the ATD circuit to the decoder. In which address line A1 has low level for all the time and a pulse generated due some noise or parasitic capacitance introduce in the circuit. it is recognized as the wrong address “01” which should not be detected by the decoder. And due to that wrong address detection the data store in the cell 2 is changed which is shown by output of cell 2 (Q2). Now, Figure 4.2 shows the response with introducing the ATD circuit. Now in this circuit it is observed that the D2 RD is not go high for the row decoder address input combination of “01” and the status of cell 2 not changed. So the wrong address which generated in the previous circuit is eliminated by introducing the ATD circuit in the decoder which avoids the wrong data to be writing to the second cell of SRAM core. Here, by introduction of ATD circuit, any address which of the period less than 152 ns is considered as the noise and it not detected. So, for this design the address change frequency

should be less than 3.26 MHz. so, this ATD circuit is designed for the processors 8085 (8 bit) which operates on the frequency of 3.07 MHz, 8086 (16 bit) which operates on the frequency of 5 MHz and the PIC controller (PIC12F629/675 - 8 bit) which operates on the frequency of DC - 20 MHz.

## CONCLUSIONS

In this work, an ATD circuit was designed to suppress the effect of noise on the address line in cadence virtuoso environment. The ATD circuit was sound to support a address change frequency up to 3.26 MHz. The testing was done on a 4\*4 asynchronous SRAM core and the functionality of the circuit was successfully verified. The test circuit of 4\*4 SRAM core was also designed in same environment. All the simulations were done for 180 nm technology node.

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