NANOPARTICLE BASED CHARGE TRAPPING MEMORY DEVICE APPLYING MOS TECHNOLOGY: A COGNITIVE APPROACH USING POLYVINYL ALCOHOL CAPPED ZINC OXIDE NANOCRYSTAL

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Abstract

Development of 'data storage device' using semiconductor based technology has always been gaining significant interests from the researchers engaged in this field. The scope of research in this field was further enhanced by the introduction of nano particle based techniques. Metal-Oxide-Semiconductor (MOS) structure provides the primary guidance in developing such devices. Design of a low cost nano particle based 'Charge trapping memory' device will be described which is expected to have superior characteristics than the conventional ones. The basic idea behind the proposed device is to find out a way to replace the continuous polysilicon floating gate of the flash cells with discrete nano crystal layer by using a Polyvinyl alcohol (PVA) capped ZnO nano particles. The basic structure of the memory cell is analogous to the charge trapping MOS transistor except the charge trapping layer being replaced by discrete nano particles. This will allow reducing the thickness of the tunneling oxide without effecting the endurance, reliability and performance of the device.

Index Terms *— Data storage, Metal-oxide-Semiconductor, Zinc Oxide, Charge trapping*

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1. INTRODUCTION

FABRICATION of memory device for 'data storage' has always been considered as an important research objectives and that leads to development of several data retention techniques.[1] Use of semiconductor based technology for the purpose has introduced a newer dimension to research activities in this field. Nowadays to develop a data storage technique the factors like 'Retention Period', 'Endurance and Reliability', 'Rate of data Transfer', 'Cost of Storing per bit data' etc. are always taken into account for effective commercialization. More powerful portable electronic devices are currently on high demand and the traditional high density semiconductor memories need to be modified further for better efficiency and to design cost effective electronic component.

The state-of-art high density semiconductor memories like DRAM allows fast write and erase in the range of 100ns or less.[2] Of course, the fact that every DRAM cell requires a large storage capacitor can be considered as a disadvantage for developing portable devices. Usually it has been observed that memory device developed for various electronic devices are silicon based and lot many research activities are still underway to develop newer devices based on this.[1],[3] The most widely used form of memory device is the floating gate type flash memory device and the pace of development of the device is far more than the expected.[4] Problem with such kind of memory device is that these are accompanied with certain limitations like limitation on device scaling, interference, charge leakage, tolerance of the material of the device etc. Therefore the focus of many research activities is now directed towards development of charge trapping memory devices. [5] The introduction of Metal Oxide Semiconductor (MOS) based technology for development of memory devices has lead to significant growth of various data storage devices such as 'Floating Gate memory device' 'Charge Trapping memory device', 'Charge Coupled memory device' etc. Semiconducting oxides such as Zinc oxide are often proposed as potential nanomaterial for development of nonvolatile memory devices due to their large band gap. Use of polyvinyl alcohol capped Zinc oxide nanoparticle may find greater significance still since PVA capped ZnO nano particles have greater band gap than ZnO nano particles. The basic motivation behind the proposed memory device is based on these facts. Nonvolatile memory devices involving metallic/semiconducting naonparticles as charge trapping element are promising in the sense that the trap level and size can be determined precisely by controlling the nanoparticle species, density and size. [6] Extensive research work in this field is expected to produce exciting results in near future.

2. METAL-OXIDE SEMICONDUCTOR (MOS)

Metal-Oxide Semiconductor (MOS) based technology for 'data storage device'

Semiconductor memory can be divided into two main types, both based on CMOS technology, volatile and non-volatile memory.

The soul of the semiconductor memory lies in the capacitance offered by the oxide layer of the MOS structure. The storage of charge (holes or electrons) in the oxide layer can be realized by applying suitable biasing to the gate, source and to the drain terminals. Figure-1 provides a schematic representation of realization of memory (charge storage) using basic MOS structure. Although the retention period of this basic device is very small, but it paved the way for future memory devices – including the flash memory cell as well as nanoparticle based memory cell.

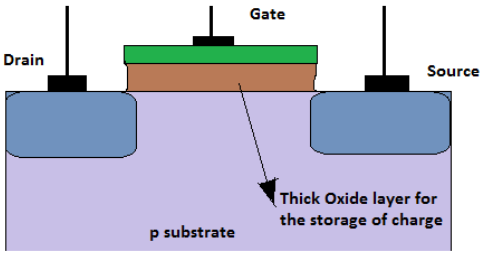

Figure-1: Schematic diagram showing the realization of memory (charge storage) using basic MOS structure.

Most of the semiconductor non-volatile memory used today are referred to as flash memory. The name is derived from the way in which cells are erased in an array (a large number of cells are erased at once). Other types of semiconductor non-volatile memory are ROM (Read Only Memory), EPROM (Electrically Programmable ROM) and EEPROM (Electrically Erasable and Programmable ROM). Flash memory developed from these were based on the fact that its programming and erasing mechanisms are appropriate and can be operated easily.

3. NANOPARTICLES

Use of nanoparticles for design of memory devices

Use of nanoparticles for memory device has greatly been encouraged in recent days because of the fact that when we use gate dielectrics embedded with nanocrystals the charge leaking to the tunneling oxide layer is reduced significantly and thus enhances the retention period of the device. Demonstrative evidences are available in literature to explain the novelty of such devices and currently significant research activities in this field are underway.[7] Quasi nonvolatile Metal Oxide Semiconductor (MOS) memory devices are known where Silicon, Germanium and Tin nanocrystals are used for charge storage. These devices possess commendable data retention properties. Of course the limit of the gate oxide layer thickness many times restricts the use of such devices.
Floating-gate layers embedded in gate materials are thus known to have extensive application as important components in nonvolatile memory applications. Among these, floating gate memory devices comprising of discrete nanocrystals have received considerable research interest in recent days due to their excellent memory performance as well as high scalability. Of course, the performance of such devices depends on the band gap of the metal and semiconductor being used. The induced interface charge in the MOS Capacitor is closely related to the shape of the electron energy bands of the semiconductor near the surface as shown in the Figure 2. The use of nanocrystals in place of continuous floating-gate in the memory devices offer faster write/erase speeds, lower power consumption, and more powerful endurance characteristics, compared to conventional nonvolatile memory devices.

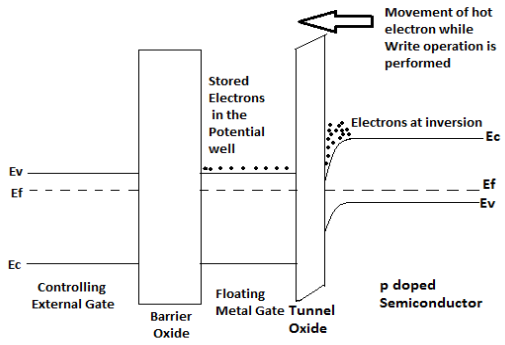

Figure-2: Schematic band diagram in n-channel floating gate MOS transistor during WRITE operation

The use of Nanocrystal as charge-storage sites embedded within the gate dielectric increase the retention time and it has been found that it is longer than as expected from floating gate device. The charge trapping/release in the nanocrystal leads to a shift in the flat band voltage. The possibility of a charge-storage memory device which exceeds the performance limits of a conventional floating gate device has attracted a great deal of interest and is spurring rapid progress in this area. Available literature reports about the nonvolatile memory devices utilizing CdTe and CdTe-CdSe nanoparticles embedded in a PVK layer obtained through spin coating technique. The C-V (Capacitance-Voltage) characteristics of the devices at 300 K under sweep voltages from −5 to 5 V showed hysteresis behaviors with a large flatband voltage shift due to the charges captured in the CdTe and the CdTe-CdSe nanoparticles, indicative of a memory effect in the nonvolatile memory devices. The magnitude of the flatband voltage shift was significantly affected by the injected area of the CdTe and the CdTe-CdSe nanoparticles. For a writing voltage of −5 V,

an erasing voltage of +5 V, and a reading voltage of −1 V applied for 1 s, the device with the shell layer demonstrated better performance than the device without the shell layer. [8] With their high dielectric constants and large band gap energies, thin film of rare earth (RE) oxides are expected to be promising candidates as replacement material for charge trapping layers in Flash memory device applications. The detailed discussion of the applications of Nanoparticles for Design of 'Memory devices' are beyond the scope of this article and these require a much wider discussions.

4. DISCUSSIONS

Discussions on the prospects of the projected memory device

The proposed device as stated above is based on MOS based technology where the gate structure has been replaced by a layered structure of a thin tunneling oxide, a layer of discrete nanoparticles for charge trapping and a thick control oxide layer. [Figure-3] The extremely thin tunneling oxide layer is supposed to allow tunneling of electrons towards the floating gate and the thick control oxide layer prevents escape of even the most energetic electrons during the WRITE operation. WRITE operation is realized by applying a suitable positive gate voltage and keeping the source grounded so as to allow the tunneling of the channel hot electrons towards the layer of discrete nanoparticles where they get tapped.

ERASE operation is supposed to be performed by applying a negative voltage to the gate keeping the source and the drain grounded. The applied negative bias on the gate cause holes from the substrate to tunnel towards the nanoparticles where they get recombined with the already trapped electrons. If applied negative bias is more it may cause the trapped electrons in the nanoparticles to tunnel to the substrate and get neutralized by recombining with the available holes

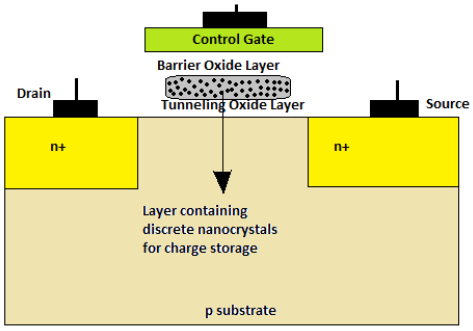

Figure-3: Schematic representation of the proposed memory device using Polyvinyl Alcohol (PVA) capped ZnS nanoparticles

As we can see in other MOS based devices, in this case also to READ the stored data, a small positive voltage is applied at the control gate. The n-channel formed at the interface will be either conducting or insulating based on the threshold voltage (governed by the amount of charge trapped in the nanoparticles) which is sensed using sensors forming a binary code thereby reproducing the stored data.

The following striking features can be expected from the proposed device:-

A. Retention Period

From the analysis of available literature we can ascertain that use of nanoparticle in place of metal might improve the retention period for the proposed device around 10 years with tunnel oxide thickness of 30 angstrom while achieving microsecond W/E time at 10V and millisecond W/E time at 6V. The use of nanoparticles in place of continuous floating gate (in Flash memory) increases the retention period to programming speed at least 1,000,000 times than the conventional Floating gate memory cell.[9]

B. Scalability

It is anticipated that the use of discrete nanoparticles for charge trapping might allow reduction in the thickness of the tunneling oxide layer and the device with 5nm oxide thickness has been fabricated.[10] Since the charges are trapped in the discrete nanoparticles even a pinhole in the tunneling oxide won't cause all the trapped to leak off and the defect will be highly localized. This reduction in the oxide layer allows the shrinkage of the device thus more number of memory cells can be fabricated on the given chip. This helps to increase the storage capacity manifold.

C. Programming Speed and Device Performance

The reduction in the physical thickness of the Oxide layer increases the overall speed during the WRITE, READ and ERASE operations. This in turn increases the overall performance of the device allowing the data transfer to be much more rapid.

D. Endurance and Reliability

With the reduction in the thickness of the tunneling oxide layer, the voltage requirement is considerably reduced up to 5V for both WRITE and ERASE operations. This reduction in the operating voltage reduces the stress on the tunneling oxide layer (reducing material degradation) which increases the life of the device. In other words, the number of WRITE, ERASE and READ cycles permitted for the device increases manifold.

E. Size of the Nanoparticle

For larger tunneling current and fast programming speed use of bigger nanocrystals are required because smaller nanocrystals may reduce the tunneling current density so as to prevent the next electron cross the barrier of the tunneling oxide.

F. Replacing Tunnel Barrier Oxide by HfO2 [11]

We are specifically advocating the use of HfO2 in place of SiO2 for higher programming speed as well as retention period, without affecting the retention characteristics keeping in mind the dependence of both on tunneling current passing through the very thin oxide layer. SiO2 based conventional devices are found to suffer from this type of limitations. Replacing the traditional SiO2 layer by HfO2 has brought superior data retention and endurance up to 1,000,000 WRITE/READ cycles. This is due to the fact that HfO2 has lower electron barrier height than SiO2. At the same time HfO2 has comparably larger physical thickness.

Thus during the WRITE operation applied bias on the gate decreases as the barrier height is reduced, so material degradation is sharply reduced. Also the larger physical thickness considerably reduces the probability of back-tunneling increases the retention period and the reliability of the device.

CONCLUSIONS

From the overall discussions it is anticipated that the proposed memory device is expected to be an efficient device compared to other devices reported so far. Further, this might significantly improve the retention period as well as programming speed of the proposed device. This is expected because use of thinner tunnel oxide is proposed for the device and additionally use of nanoparticles is expected to dramatically improve both the factors namely the 'Retention Period' and 'Programming Speed'. Another important aspect of the proposed device is that it is expected to operate at lower voltage which might ensure enhanced reliability and life of the device.

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