FPGA IMPLEMENTATION OF RACE CONTROL ALGORITHM FOR FULL BRIDGE PRCP CONVERTER

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Abstract

In this paper, the unedited race-control algorithm (RCA) for the full-bridge passive resonant commutated poles (FB-PRCP) converter is presented and implemented in cost effective field programmable gate-array. It compensates the drawbacks of that topology that are related to the slow dynamics of the auxiliary poles which are necessary to obtain zero-voltage transitions both at turn-on and turn-off conditions and makes possible its use in more general welding applications, such as manual metal arc welding, in which very fast responses are required. The proposed RCA is a simple variation of the traditional phase-shift technique, which leads to significant efficiency improvements. The guiding idea is to apply the phase-shift technique to both legs of the converter, contrarily to what has been done to date. The limitation in dynamics of the converter is completely eliminated and it gains much more readiness. The effectiveness of the RCA has been verified in simulation and it can be experimentally tested on a true converter..

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1. INTRODUCTION:

Most resonant switching topologies are not optimal for welding power supplies (WPS) due to the very wide variation of load currents (typically 3 % to 100 %). A possible remade is to employ additional resonant poles as done in Pseudo resonant full bridge converter (PRFB), the passive resonant commutated pole converter (PRCP) and the auxiliary resonant commutated pole converter. The typical welding power supply is given in Fig. 1.

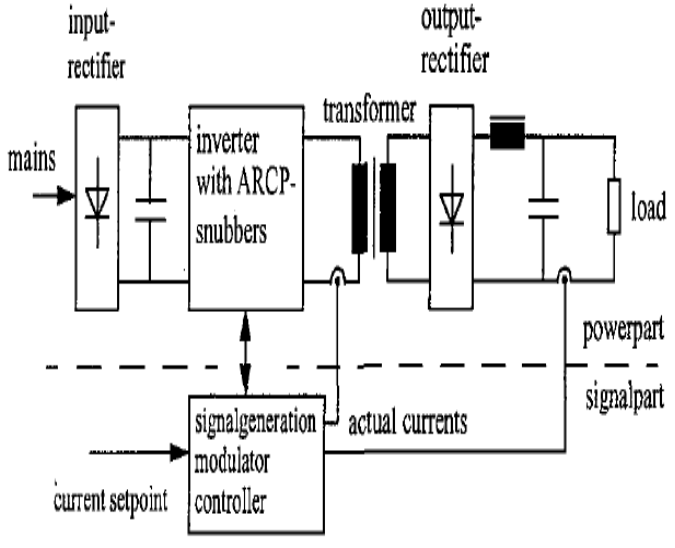

Figure – 1: Typical Welding Power Supply

In the general scenario of the switching converters for welding applications, many efforts have been done so far to convert significant power while minimizing costs and overall dimensions, hence, power dissipation. The degrees of freedom to achieve these goals are the switches' performance and the converter topology. In fact, while the semiconductor technology goes on in lowering the ON-state losses and the commutation losses of the switches, the power-electronics technology proposes newer and newer and more efficient topologies, including refined-control strategies, aimed to achieve soft switching for the devices of the circuit at input and load ranges as wide as possible.

On the side of the power switch's development, a state of-the-art survey on the performances of the classical soft switching phase-shift bridge topology has been presented in [1], where the authors demonstrated that, depending on the switches used in the circuit, some load conditions are more critical in terms of the device's reliability than other ones.

On the other side, in the field of research of new topologies for welding converters, many circuits have been proposed in the past based on hard-switching techniques [2]–[4] that allow a simplified control strategy due to the intrinsic absence of resonance transients, whose duration is affected by the load conditions. The unavoidable drawback of these topologies is the switching losses, which severely limit the frequency, hence, the physical dimensions. Many innovative topologies belonging to the soft-switching category have been developed. Series-resonant topologies [5], [6] have been proposed and tested for welding applications, in which one- or three-phase mains supply a classical H-bridge isolated converter. Soft-switching conditions are achieved owing to a resonance that involves a series capacitor. These kinds of topologies, though, offer an

additional voltage drop across that capacitor that forces the designer to reduce the transformer's ratio and, in turn, to adopt over dimensioned secondary rectifiers in terms of blocking voltage. Another kind of soft-switching topology, presented in 2001, contemplates the presence of an auxiliary transformer whose rule is to obtain zero-current-switching conditions for the main leg of the inverter in a wide range of load conditions [7]. That auxiliary transformer, indeed, requires a powerful controller to evaluate the optimal dead-times required to obtain soft-switching conditions. A simpler topology has been presented in 2006 that provides zero-voltage-switching (ZVS) conditions for each switch of the circuit [8]. Its main drawback is that a half-rail dc voltage is required, which is often very difficult to obtain. Similarly, in the same year, a very efficient topology has been developed and presented [9], whose primary drawback is the half-bridge configuration, which provokes high current stresses to the main capacitors causing reliability problems.

A soft-switched topology, called pseudo resonant full-bridge dc/dc converter, has been introduced in [10]. The basic principle of that solution is to use a reactive circuit to obtain ZVS at each load condition. The same principle was enhanced and adopted in 1997, when Frohleke et al. [11] presented an implementation of a circuit called full-bridge passive resonant commutated poles (FB-PRCP), which is fully zero-voltage transition (ZVT), and demonstrated its application to a power converter rated at 12 kW, 350 A. An analogous topology was presented in 1999 by the same authors [12]. The scheme of the converter presented in [11] is shown in Fig. 2. The operation principle is as follows: the two legs A and B are commutated with a classical phase-shift technique, i.e., each of them has a duty cycle of 50%, and the primary winding of the transformer receives increasing power at increasing delays ("phase shifts") of leg B with respect to leg A. The maximum power transfer is reached when leg B is 180◦ delayed from leg A, and a null transfer is obtained when leg B is in phase with leg A.

The soft-switching operation is intrinsic at the turn-on for each phase-shift topology, being the switches turned on when the reverse diodes are conducting. Soft turn-offs are obtained in this topology in a classical way: Four snubber capacitors are put in parallel to the four switches, namely, CAp, CAn, CBp, and CBn. As it is known from the literature [13], this solution is generally good for heavy and medium loads, where the stray inductance of the transformer's primary winding is energized enough to completely charge and discharge those snubber capacitors, but it is dramatic at light loads, where the magnetization is not sufficient to perform the whole leg commutation, and the switches are fired on a still-charged capacitor, in a manner very similar to a short-circuit turn-on.

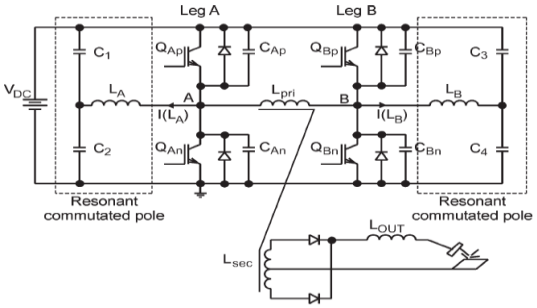

Figure – 2: FB-PRCP converter

To solve this problem, many authors have recently adopted several solutions [14]–[16]. The authors of [11] proposed an interesting and cheap solution to ensure a minimum of the switches' current values, which includes an auxiliary reactive network made up of the inductance LA(LB) and the capacitors C1 and C2 (C3 and C4) for leg A (leg B). Referring to Fig. 2, the principle of operation is as follows: due to the fixed duty cycle of legs A and B to 50%, each inductance LA and LB is subject to a square-wave voltage drop, whose amplitude and frequency are constant. At steady state, the average currents into LA and LB are zero, and the currents' peak are symmetric with respect to zero and correspond to the leg commutation.

For this reason, the current flowing into the switches at the commutation instant has a minimum value, which ensures the completion of the commutation from one rail to another and, hence, ensuring a reasonable upper limitation to dead-times. This profitable behavior allows one to use fixed-dead-times generators, thus largely simplifying the design of the modulator.

Fig. 3 shows the typical waveforms of an FB-PRCP converter. Switches belonging to the same leg are driven by opposite signals, except for the dead-times, which are necessary to avoid a leg short-circuit. The primary winding of the transformer is subject to an effective voltage V (A)−V (B), which depends on the phase shift, i.e., the delay of leg B from leg A. By varying this quantity, it is possible to regulate the power transfer to the secondary winding and, eventually, to the load. Fig. 3 also shows the triangle-shaped current waveforms into the auxiliary inductances.

Even if Frohleke et al. [11] demonstrated that it is possible to design the auxiliary poles in such a way to obtain ZVT at each load conditions at steady state, some malfunctions happen when the phase shift is considerably varied. Such a condition is very typical for manual metal arc-welding (MMA) applications, where very frequently, a fusion droplet causes the collapse of the load impedance and a drastic power-transfer reduction is required in few switching periods.

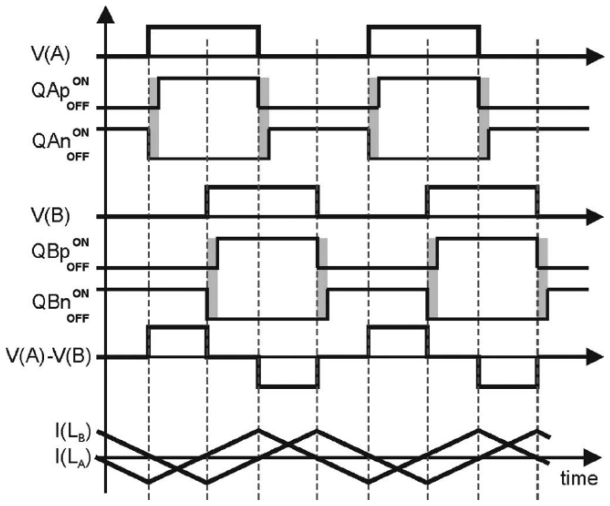

Figure- 3: Typical waveforms of the FP-PRCP converter. (Shadowed Dead-times)

To fix the ideas, Fig. 4 shows the scenario in which the phase shift is reduced from 90% (about 160◦ delay) to 25% (45◦ delay). In that figure, the leg voltages, V (A) and V (B), and the currents of the auxiliary inductances, I(LA) and I(LB), have been reported. In this case, the commutation of leg B is anticipated when the current into the inductor LB is still positive (arrow in Fig. 4), thus not allowing the normal ZVT of the leg voltage and, eventually, provoking a disastrous turn-on over a capacitance, which is very similar to short-circuit conditions.

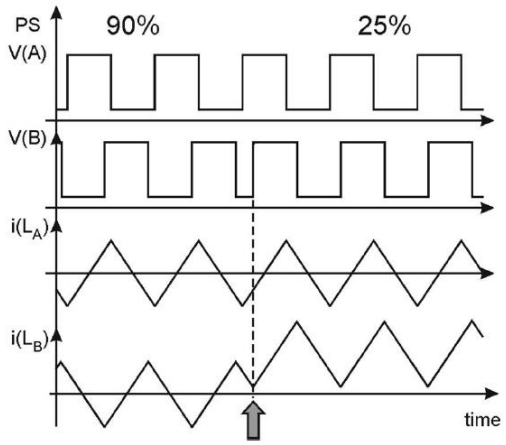

Figure – 4: Critical leg switch due to a phase-shift reduction (90%–25%). The arrow shows the abnormal condition.

For these reasons, until now, the FB-PRCP topology has been concretely employable only in welding applications with slowly variable output currents, such as gas metal arc welding and MIG/MAG processes, and, in any case, it adopts a large and expensive output inductor that slows down the fast impedance transients of the load, thus also limiting the system readiness.

Owing to the introduction of field-programmable gate arrays (FPGAs) and, in particular, to the recent advances in FPGA applications for power conversion [17], it is possible to implement complicated control algorithms at affordable—if not negligible—cost/performance ratios.

In this paper, an FPGA-based modified control algorithm called race-control algorithm (RCA) is presented, that completely eliminates the limitation in phase-shift transients, like the ones shown in Fig. 4, and significantly improves the bandwidth of the FB-PRCP topology. Some noticeable advantages are that the converter is much more ready and becomes good also for MMA welding, and the needed output inductance could be significantly smaller, hence, cheaper.

Moreover, in perspective, owing to the more and more FPGA cost reduction, the possibility of implementation of the whole converter's control algorithm in a single FPGA chip could be considered.

2. PRINCIPLE OF OPERATION OF THE RCA

The RCA principle descends from the following observation: In the classical approach, leg A is a fixed frequency and phase, whereas leg B is shifted ahead and backward. In this way, phase-shift reductions are achieved by anticipating that leg, which might cause dramatic commutations, whereas phase shift increases, achieved as a delaying of the same leg, result as always safe. This observation suggests a modification of the control algorithm as follows: Leg B is delayed when an increase in phase shift is needed, whereas leg A is delayed when a reduction is needed instead. In this way, each leg is never anticipated, and the scenario of Fig. 4 is completely avoided.

To show the effectiveness of the principle stated earlier, the worst case is shown in Fig. 5, where a sequence of three switching periods at extreme phase-shift variations (0% → 100%(180◦) → 0%) has been depicted. In that figure, the same signals of Fig. 4 have been reported, together with the primary voltage of the transformer V (A)−V (B) and the magnetization component of the primary current of the transformer. This latter quantity is primary to study the transformer's saturation.

From the point of view of the safeness of the commutations, the problem shown in Fig. 4 is completely solved. Each commutation happens at a safe status, in which the auxiliary inductances are magnetized at a proper current.

Fig. 5 also shows that the RCA approach exhibits a drawback. The current peak of the inductor belonging to the delayed leg is increased. Its value can be evaluated as follows:

$$\Delta_i\left(L_A\right)_{Peak} = 2\frac{\Delta T}{T}\Delta_i\left(L_A\right)_{Peak} = \Delta PS\%\Delta_i\left(L_A\right)_{Peak} \quad \text{-- (1)}$$

where Δi(LA)peak is the inductance peak-current increase, T is the switching period, ΔT is the period variation, and ΔPS% is the phase-shift variation. In the extreme scenario of Fig. 5, Δi(LA)peak reaches 2· i(LA)peak (100% increase).

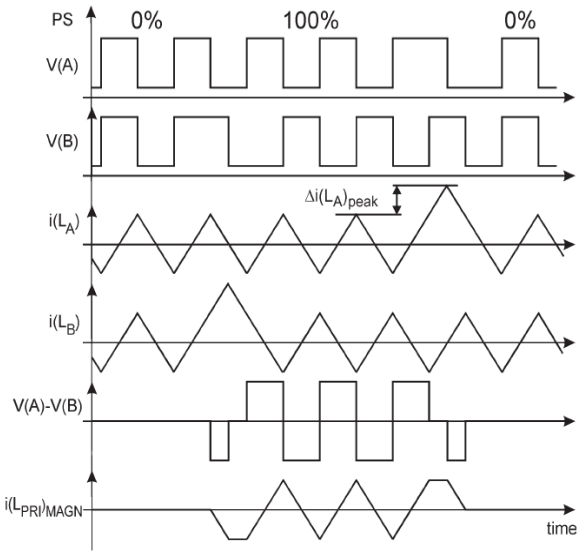

Figure – 5: Safe leg commutations in correspondence of an extreme phase-shift transition (0% → 100% → 0%)

However, this peak increase is not critical from the switch losses' point of view nor from the transformer's saturation one. In fact, according to the design consideration illustrated in [10], the resonant commutating-pole currents i(LA) and i(LB) are much lesser (few percents) than the primary currents at heavy loads so that the switches can also easily tolerate a doubling in those currents. In addition, it is reasonable to assume that the events of heavy variations of phase shifts (0% → 100% variations) are relatively rare in the switching-frequency time scale. Finally, ZVTs are always performed in this topology, thus hugely compensating those over currents from the point of view of the switches' stresses.

For what concerns the effects on the transformer's saturation, the lower trace of Fig. 5 has been obtained by time-integrating the voltage across the primary winding V (A) − V (B). Its shape easily demonstrates that the maximum of the magnetization current, corresponding to the maximum magnetic flux of the transformer, is not affected by the RCA technique at all.

The core of the RCA is a choice: it is delayed leg A or leg B depending on the sign of the phase-shift variation. The chosen leg is delayed by a factor equal to one half of the phase shift variation. For example, a phase shift increase of 100% corresponds to a delay of leg B equal to 50% of the period (180◦). The flow chart of Fig. 6 describes this modus operandi. It is worthwhile to note that, due to the algorithm structure, simultaneous leg delays are intrinsically impossible.

3. PROPOSED FPGA IMPLEMENTATION

Having the RCA based on a difference, to avoid possible communication errors between the external controller and the modulating logic, that could result in a catastrophic misalignment of the desired and the real phase-shift values, it must be implemented in FPGA logic in such a way that the required operations of the algorithm are made inside a unique chip.

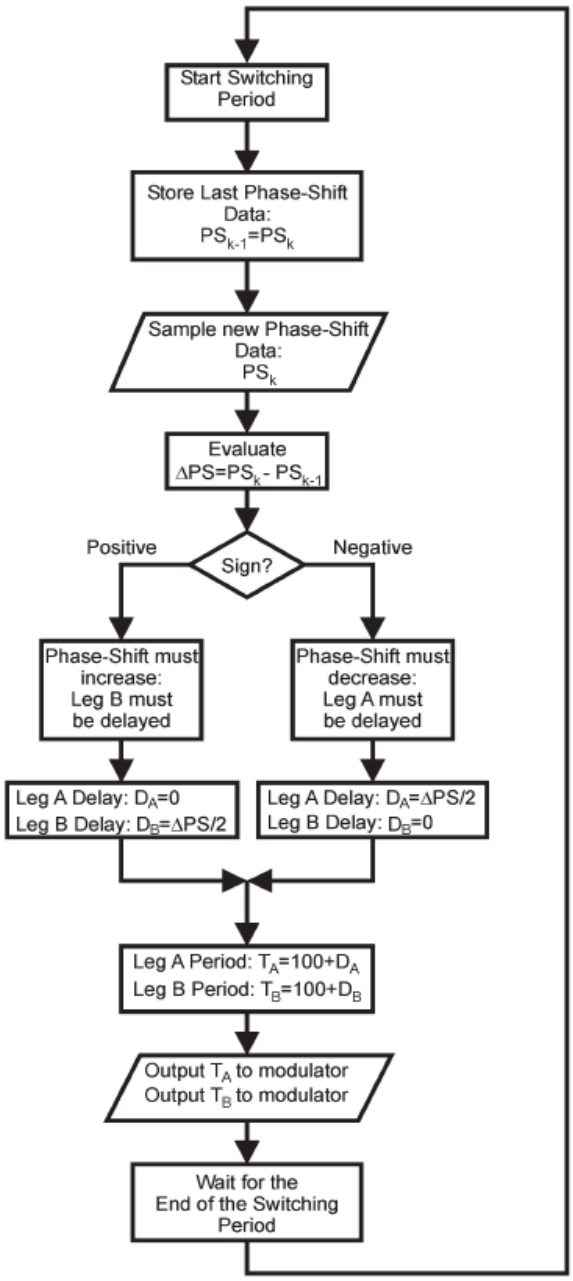

Figure – 6: Flowchart of the RCA algorithm

The second stage evaluates the phase-shift variation and its opposite in such a way as to always obtain a positive result. Two 8-b subtractors simultaneously perform the two possible subtractions between the present and the past phase-shift data.

Their outputs are

for leg A, $S_{A,K} = PS_{k-1} - PS_k$ --(2)

and

for leg B, $S_{B,K} = PS_k - PS_{k-1}$ --(3)

where k is the present time instant and k − 1 is the past one.

The third stage implements the core of the algorithm: It determines which one of the two legs must be delayed, depending on the sign of the phase-shift variation. In more detail, its outputs are

$$\Delta S_{A,K} = \begin{cases} S_{A,K} & if\ S_{A,K} \geq 0 \\ 0, & if\ S_{A,K} \angle 0 \end{cases} \quad --(4)$$

$$\Delta S_{B,K} = \begin{cases} S_{B,K} & if\ S_{B,K} \geq 0 \\ 0, & if\ S_{B,K} \angle 0 \end{cases} \quad --(5)$$

for legs A and B, respectively. In other words, the function max (Sk, 0) is implemented for each leg. To achieve this result, for leg A, the borrow signal of the subtractor is used by a two way 8-b multiplexer to choose between zero (00h in Fig. 7) and the phase-shift increase SA,k. An identical circuit is adopted for leg B. For example, if the phase shift increases, PSk is greater than PSk−1, then SA,k will be negative (borrow = 0) and SB,k will be positive (borrow = 1). This result will provoke the multiplexer of leg A to choose 00h and the corresponding one of leg B to choose SB,k. Eventually, leg B will be delayed, and leg A will be kept at constant phase, as expected from the algorithm discussed in the previous section.

The fourth stage has a trivial role. It operates the divisions by two, which are necessary to scale the phase-shift quantities, in the range 0d–100d to the delay quantities which are in the range of 0%–50% (it could be useful to remember here that the maximum phase shift is obtained at delays of 50% of the switching period, which correspond to a phase delay of 180◦). These divisions are simply obtained by right-shifting the result of the previous stage by one. Of course, the precision is worsened from 1% to 2%. In general, this value is still acceptable for this kind of application. If not, it is very simple to operate the phase-shift data in the range of 0d–200d instead of 0d–100d to obtain back the 1% precision.

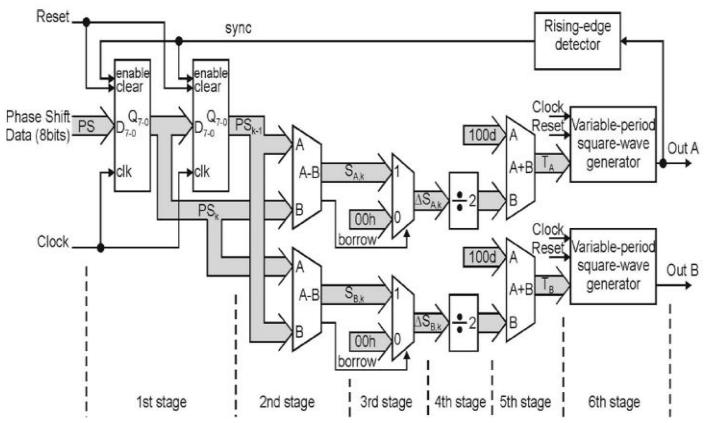

Figure - 7: Top-level schematic of the FPGA implementation

The fifth stage composes the period time of the switching waveform for each leg. At steady state, the period is equal to 100d. When one leg must be delayed, its period must be increased of the previously calculated quantities. In

$$T_A = 100d + \frac{\Delta S_{A,K}}{2} \quad --(6)$$

$$T_B = 100d + \frac{\Delta S_{B,K}}{2} \quad --(7)$$

where TA and TB are the durations of the next periods of legs A and B, respectively. An unsigned 8-b adder is used for each leg at this stage. No overflow conditions are possible, being the maximum output period given by (6)

$$T_{A,\max} = 100d + \frac{100d}{2} = 150d \quad --(8)$$

which is representable with 8 b. Please explicitly note that, at each switching period, the leg which is not being delayed is forced to T(fixed leg) = 100d.

The sixth stage is the modulator. The two square-wave generators of Fig. 7 produce a square-wave period with duty cycle D = 50%, whose period is variable, and the new period value is sampled at the end of each cycle.

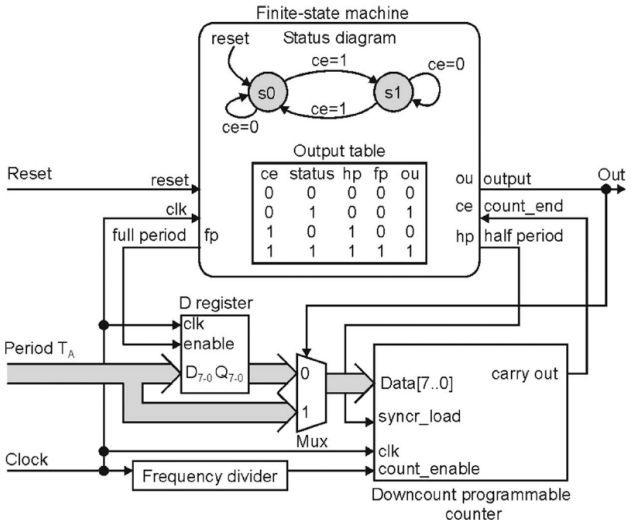

Figure – 8: Schematic of the variable-period square-wave generator

Fig. 8 shows the block diagram of one generator. A simple finite-state machine (FSM) controls a buffer (D-register), which contains the present period value, a multiplexer, and a loadable down-counter. A frequency divider provides the necessary clock frequency division to obtain the desired switching frequency. In the experiment section, a switching frequency of fS = 15 kHz has been used, and being the half-period at steady state equal to a count value of 100d, it is easy to calculate the countdown frequency as

$$f_{COUNT} = f_S \cdot 2 \cdot 100d = 3M\ Hz \qquad \text{--(9)}$$

The main clock of the FPGA oscillates at 48 MHz, so the frequency divider's ratio in Fig. 8 is 48 MHz/3 MHz = 16.

The FSM operates between two statuses, s0 and s1, corresponding to the output statuses of 0 and 1, respectively, whose mode of operation is described as follows. Please note that the circuit operates at main clock frequency, including the syncr_load signal of the counter. Due to the input count_enable, the countdown, instead, takes place at reduced frequency [(9)].

To fix the ideas, suppose that the FSM was in the s1 status and that the counter asserted the count_end signal in the last clock period, thus making the FSM to switch to the status s0. In this condition, the multiplexer is set to the input TA, and the FSM asserts both the half-period and the full-period signals, thus loading the counter with the new period value TA and latching it also into the D register. The countdown starts. Having the FSM in the status s0, the Out signal is kept to zero, and nothing happens until the count_end signal is asserted. After TA counts, corresponding to half-output period, the countdown ends, and the signal count_end is asserted again. In this case, though, the FSM asserts only the half-period signal, thus making the counter to be reloaded at the same value TA, which is stored into the D register. The full-period signal, instead, is not asserted in this case; in such a way, the "one" time is forced to be of the same duration of the "zero" time. The FSM switches to its s1 status, and a new countdown starts. During the second countdown, the signal Out is kept to one. At the period end, the full_period signal is asserted, thus provoking the acquisition of the new period data.

The behavior of the modulator circuit in Fig. 7 is as follows: At a new period start (rising edge) of the signal OutA, the D registers shift, and a new phase-shift PSk data is acquired. At this point, two cases must be considered: PSk = PSk−1 and PSk _= PSk−1. If PSk = PSk−1, then both the subtractors of stage two produce zero, both the multiplexers of stage three produce zero, and the same for the dividers of stage four, so that the adders of stage five produce both TA = TB = 100d, which is exactly the switching period, and the square-wave generators of stage six go on to produce two square waves at locked phase.

If PSk _= PSk−1, the signal SA,k and SB,k are opposite in sign [(2) and (3)]. To fix the ideas, suppose that PSk < PSk−1 (hence, SA,k > 0 and SB,k < 0). In this case, the upper multiplexer at stage three sees a borrow signal equal to one and outputs ΔSA,k = SA,k [(4)], whereas the lower one sees a borrow equal to zero and zeroes its output ΔSB,k [(5)]. After the division by two of stage four, the adders of stage five produce TA = ΔSA,k/2 + 100d [(6)], y and TB = 100d [(7)]. In this way, leg A is driven by a slower oscillation period and delays with respect to leg B, according to the behavior described in Fig. 6. Of course, if PSk > PSk−1, leg B is delayed instead. It is worthwhile to explicitly note that, if the new phase shift value is kept constant at the following period, everything behaves like the earlier case PSk = PSk−1, and the oscillation period of leg A intrinsically returns back to TA = TB = 100d, thus keeping leg A indefinitely delayed until a new phase-shift variation occurs.

As a final consideration about the behavior of the proposed circuit in Fig. 7, it can be useful to note that, due to the shift of leg A, the sync signal which governs the phase-shift acquisition is not strictly periodic. In fact, it is delayed each time a phase-shift reduction occurs (in that leg A is delayed), up to a 50% of the switching period. Even if this behavior could cause some additional troubles in the design of the external controller, particularly if this one implements a constant time step algorithm, it is useful to consider that this delay is typically very small, due to the slow phase-shift variations required in normal operations, and, anyway, in the worst case, it is limited to a maximum of half a period, thus keeping locked the external controller frequency with the modulator's one.

4. SIMULATION RESULTS:

The Quartus II developing environment by ALTERA Corporation [18] has been adopted to simulate and to implement the presented system, and the two devices used for the experimental part have been summarized in Table I. There, the total resource usage, in absolute and percent units, has been reported together with the estimated commercial cost of each device.

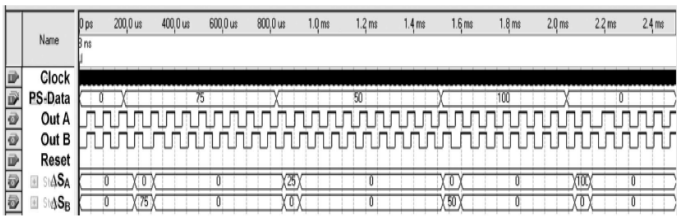

Figure – 9: Quartus II logic simulation of the RCA algorithm

Following the approach bottom-up, the single parts of the design have been implemented into the Quartus II environment and have been tested by means of the timing simulator.

The simulation of the overall system has been shown in Fig. 9, in which the output signals are included together with the PS-data and the intermediate signals ΔSA and ΔSB in Fig. 7. The clock signal is too dense in this time scale to be displayed. At the simulation start, a Reset signal of the duration of one to two clock periods is given to the system and is not visible. Initially, PS-data is kept to zero. At 200 μs, the PSdata is changed to 75d. At the rising edge of OutA, the new data are sampled, and the stages one to three in Fig. 7 correctly compute the values of the signal ΔSA and ΔSB. In fact, in the transition 0d → 75d, being the variation positive, leg B has to be delayed (ΔSB = 75d) and leg A does not have to change (ΔSA = 0). These values are immediately supplied to the square-wave generators that adequate their periods. Specifically, the output OutB performs a longer period at about 300 μs and, at steady state, it keeps its delay until the new transition. It is worthwhile to explicitly note that signals ΔSA and ΔSA differ from zero for one period only. This is correct, because the data at the last time PSk−1 have become equal to that at the present time PSk (see Fig. 7). Nothing changes until the next transition at about 850 μs. In this case, a phase-shift reduction is required, and ΔSA differs from zero. The signal OutA is slightly delayed, and the phase shift reduces to the appropriate quantity.

Further transitions are stimulated at 1500 and 2100 μs, and the phase shift is finally returned back to zero. The system always produces the correct response at each condition.

The RCA has been tested on true prototype inverter equipment, of a scaled size in terms of voltage and currents, whose main parameters are summarized in Table II. In addition, a large simplification has been done by substituting the secondary stage of Fig. 2 with a fixed-value resistor to better evaluate the behavior of the primary stage independently of the second order effects introduced by the secondary freewheeling currents and diode reverse recovery.

CONCLUSIONS

Due to the rising demand for portable volume, weight and cost reduced welding power supplies in the mid and high power range the passive resonant commutated pole converter is inspected for wide load range applications. The availability of cost effective digital solutions such as FPGA and power supply modules facilitates the application of Passive resonant commutated pole converter to ever lower power levels.

An unedited control technique called RCA for FB-PRCP converters has been implemented on an FPGA platform and successfully experimented thro simulation.

The technique promises to strongly improve the dynamic responses of high-power FB-PRCP converters used in welding applications, thus allowing reduction of the heavy and expensive output inductances and/or to perform an advanced control of the welding current shape which is typical for MMA applications.

The adoption of the presented technique is of course strictly related to the possibility of using digital control circuits, like FPGAs, although whose supplementary cost is largely compensated by the economies of passive components.

Verification of above proposed algorithms are given by simulations and measurements are resenting a basis for further development.

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