DESIGN OF LOW POWER 4-BIT FULL ADDER USING SLEEPY KEEPER APPROACH

B. Srujana Sri[1], B. Saraswathi[2], G. Arun Kumar[3], A. Bhav Singh[4]

[1,2,3]Student, [4]Assistant Professor, Department of ECE, SITS (KHAMMAM), AP, INDIA, ***bandisrujana@gmail.com, ananya.saru@gmail.com, geejula.arun@gmail.com, subhakararao.408@gmail.com***

Abstract

ITRS reports that leakage power dissipation may come to dominate total power consumption. A novel approach, named "sleepy keeper," which reduces leakage current while saving exact logic state is presented in this paper. In the design of VLSI Circuits, the transistor length is rapidly scaling down. Due to this the leakage power dissipation has become an overriding concern. Sleepy keeper uses traditional sleep transistors plus two additional transistors driven by a gate's already calculated output to save state during sleep mode. Using Sleepy Keeper approach, a low power 4-bit Full Adder with only 80T is designed as it takes 112T to design conventional Full Adder. Experimental results are carried out in Electric VLSI 8.09, Power Analysis and delay in Tanner EDA.

Keywords*: - Dual Vth, Sleepy Keeper, Transistor Count, Low Power, Full Adder (FA).*

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1. INTRODUCTION

In the past major concern in VLSI design was area, performance, cost and reliability; power consideration was mostly of secondary importance. In recent years, this has begun to change increasingly; power is being given comparable weight to area and speed consideration. High Power systems often run hot; high temperature tends to exacerbate several silicon failure mechanisms. In order to achieve high density and high performance CMOS technology feature size and threshold voltage have been scaling down for decades. Because of this technology trend, transistor leakage power has increased exponentially. As the feature size becomes smaller, shorter channel length's result in increased sub threshold leakage current through a transistor when it is off. Low threshold voltage also results in increased sub threshold leakage current because transistors cannot be turned off completely. For these reasons, static power consumption has become a significant portion of total power consumption for current and future silicon technologies.

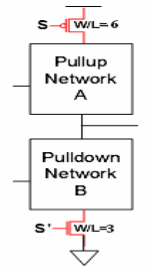
The growth of personal computing devices (portable desktops, audio and video-based multimedia products) and wireless communication systems demand high-speed computation and complex functionality with low power consumption. In this context, peak power (maximum possible power dissipation)is a critical design factor as it determines the thermal, electrical limits of the designs, impacts the system cost, size and weight; dictates specific battery type; system packaging and heat sinks; aggravates resistive and inductive voltage drop problems pointing to an ultimate solution-Low Power VLSI Technology.

There are several VLSI techniques to reduce leakage power. Each technique provides an efficient way to reduce leakage power, but disadvantages of each technique limit the application of each technique. This paper mainly emphasized on reducing the count of transistors using Sleepy Keeper approach, which ultimately reduces the power dissipation.

2. PREVIOUS RESEARCH WORK DESCRIBING DIFFERENT LEAKAGE REDUCTION TECHNIQUES:

2.1Sleep Approach:

The most well-known traditional approach is the sleep approach **[2][3].**In the sleep approach, both(i)an additional "sleep" PMOS transistor is placed between Vdd and the pull-up network of a circuit and (ii)an additional "sleep" NMOS transistor is placed between the pull-down network and GND as shown in Fig.1.These sleep transistors are turned on when the circuit is active and turned off when the circuit is idle. By cutting off the power source, this technique can reduce the leakage power effectively. However, output will be floating after sleep mode, so the technique results in destruction of state plus a floating output voltage.



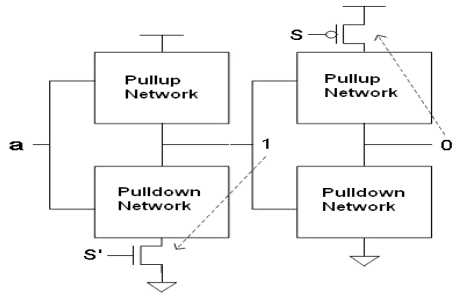
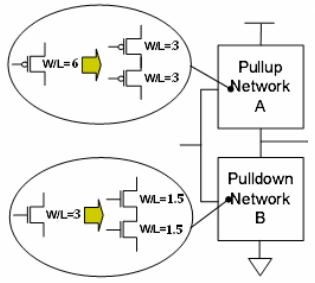


Fig.1 Sleep approach **Fig.2** Zigzag approach

2.2 Zigzag Approach:

A variation of the sleep approach is the Zigzag approach, reduces wake-up overhead caused by the sleep transistors by placement of alternating sleep transistors assuming a particular pre-selected input vector**[4]**.In Figure 2,assume that ,in sleep mode, the input of the logic is '0' and each logic state reverses its input signal, i.e., the output is '1' if the input is '0' and the output is '0' if the input is '1',then a sleep transistor is added to the pull down network; if the output is '0',then a sleep transistor is added to the pull-up network. Another technique for leakage power reduction is the stack approach, which forces a stack effect by breaking down an existing transistor into two half size transistors **[5]**; Figure 3 shows its structure. When the two transistors are turned off together, induced reverse bias between the two transistors results in sub threshold leakage current reduction. However, divided transistor increases delay significantly and could limit the usefulness of the approach.

The Sleepy Stack approach combines the sleep and stack approaches. The sleepy stack technique divides existing transistors into two half size transistors like the stack approach. Then sleep transistors are added in parallel to one of the divided transistors as shown in Figure 4.During the sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current while saving state. Each sleep transistor, placed in parallel to one of the stacked transistors, reduces resistance of path, so delay is decreased during active mode. However, area penalty is a significant matter for this approach. Since every transistor is replaced by three transistors and since additional wires are added for S and S', which are sleep signals



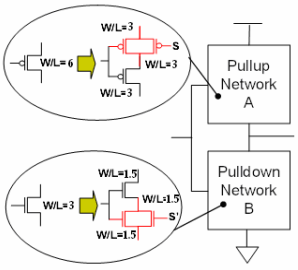


Fig3.Stackapproach **Fig4**.Sleepystackapproach

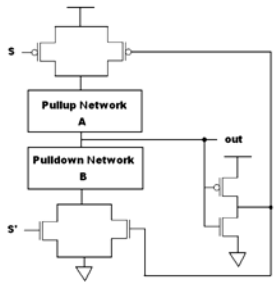


Fig.5 Leakagefeedbackapproach

The leakage feedback approach is based on sleep approach. Fig.5 shows the structure of leakage feedback approach which uses two additional transistors to maintain logic state during sleep mode, and two transistors are driven by the output of an inverter which is driven by output of a circuit implemented utilizing leakage feedback As shown in figure5,a PMOS transistor is placed in parallel to the sleep transistor(S) and an NMOS transistor is placed in parallel to the sleep transistor(S').The two transistors are driven by the output of inverter which is driven by output of a circuit. During Sleep mode, sleep transistors are turned off and one of the transistors in parallel to the sleep transistors keep the connection with the appropriate power rail.

3. PROPOSED LEAKAGE REDUCTION TECHNIQUE "SLEEPY KEEPER"

The basic problem with the traditional CMOS is that the transistors are used only in their most efficient and naturally inverting way namely PMOS transistors connected to Vdd and NMOS transistors connected to GND.It is well known that PMOS transistors are not efficient at passing GND; similarly, it is well known that NMOS transistors are not efficient at passing VDD.

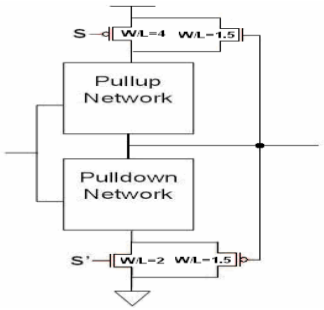


Fig.6 Sleepy Keeper Approach

However to maintain a value of '1' in the sleep mode, given that the '1' value has already been calculated, the sleepy keeper approach uses this output value of '1' and an NMOS transistor connected to VDD to maintain output value equal to '1' when in sleep mode. As shown in figure 6, an additional single NMOS transistor is placed in parallel to the pull up sleep transistor connects VDD to the pull-up networkWhen in

sleep mode, this NMOS transistor is the only source of VDD to the pull-up network since the sleep transistor is off. Similarly to maintain a value of '0' in sleep mode, given that the '0' value has already been calculated, the sleepy keeper approach uses this output value of '0' and a PMOS transistor connected to GND to maintain output value equal to '0' when in sleep mode.

4. EXPERIMENTAL METHODOLOGY

To implement this novel approach, which is "Sleepy Keeper' Full Adder is considered. The below figure shows schematic of modified Full Adder having 20T including sleep transistors. The sleep transistors are connected to the pull-up and pull-down networks respectively. Each Pair of Sleep transistor is driven by the output of the previous stage.

4.1 Circuit Operation:

Here 'A' is considered as a control signal and whatever the input is applied to the 'A' input; it is applied to both upper PMOS transistor and bottom NMOS transistor. Depending on the input signal whether it is '0' or '1', the respective device is ON and the corresponding output is used to drive the remaining circuit. When A='0', the top PMOS transistor is on and the bottom NMOS transistor is off. The Vdd which is drawn is sufficient to drive the B XOR C, B AND C circuit outputs. When A='1', the top PMOS transistor is off and the bottom NMOS transistor is on and Vdd which is drawn is sufficient to drive the B XNOR C, B NAND C circuits and produce the respective outputs. The simulation of the schematic is carried out in LT-SPICE for the condition where A='0' as well as A='1' and the waveform is shown in the above figure.

In the above figure, the sleep transistors are added to both pull-up and pull-down networks whose input is driven by the output of the previous stage. Here the input signal 'A' acts a s a control signal and the circuit operation is same as explained for previous circuit.

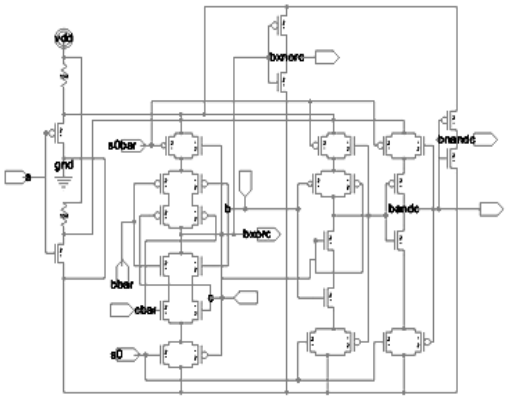


Fig.7 Schematic of 20T Full Adder with Sleepy Keeper

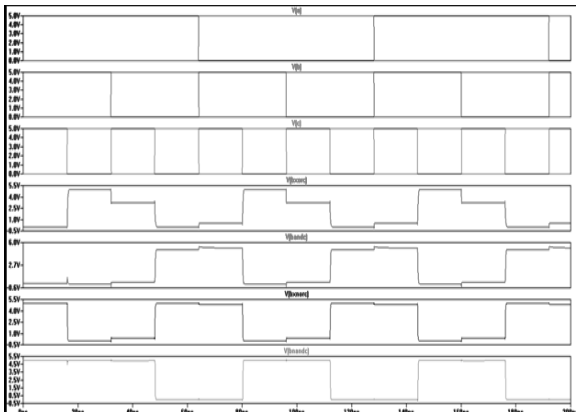


Fig.8 Waveform for 20T Full Adder with sleepy Keeper

4.2 Proposed Design of 4-bit Full adder:

The above circuit is drawn in Electric VLSI by cascading 4 1-bit Full Adders in series such that the carry out bit of the 1st Adder is given as Carry in bit for the successive stages. The waveforms are derived for each single stage but the waveform for the last stage is shown in the below figure for all the possible combinations of the input.

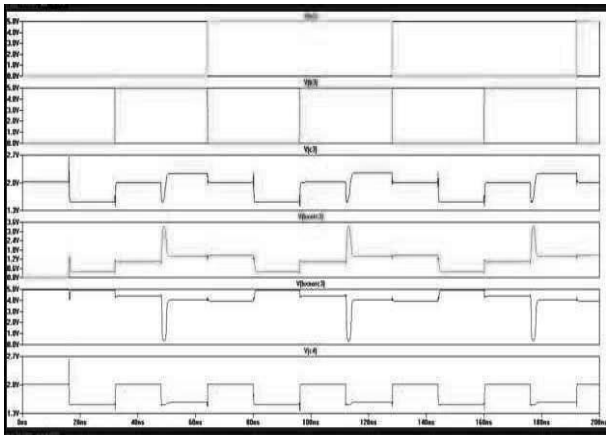


Fig 10.Waveform for 20T FA with Sleepy Keeper

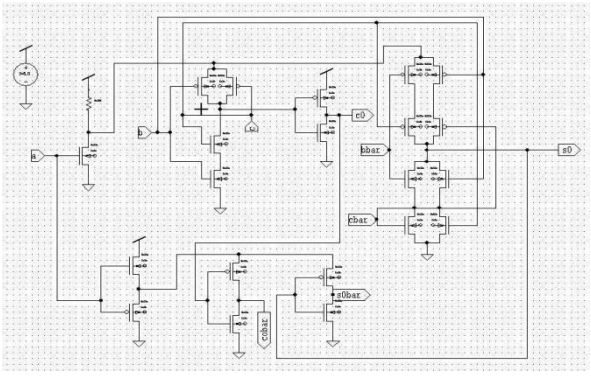


Fig11. Schematic of 20T FA in Tanner EDA

5. APPLICATIONS

1. Multiple Sleep modes like Zigzag Horizontal and Vertical Sleep Transistors are used to reduce leakage power in On-Chip SRAM peripheral circuits.
2. Intel uses sleep transistors in the design of 65nm SRAM chips which are used to shut-off the leakage in inactive sub-blocks and cut it when any of the elements of the array is accessed.

CONCLUSIONS

In order to achieve high performance and speed, the feature size and threshold voltage of CMOS technology is gradually scaling down which results in increase of leakage power dissipation. A Novel approach namely "Sleepy Keeper" which is an efficient methodology to reduce leakage power is presented. The main contribution towards this paper is to reduce the count of transistor count to 20 for 1-bit Adder and achieve less dynamic power dissipation of 15mw.

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