A LOW POWER ADDER USING REVERSIBLE LOGIC GATES

T. Naga Babu[1], D. Sounder[2], B. Subhakara Rao[3], P. Bose Babu[4]

[1, 2] *P.G. Students, Department of ECE, SITS, AP, INDIA,* ***nagababu432@gmail.com***
[3] *Assistant Professor, Department of ECE, MIET, AP, INDIA,* ***raghukanth8@gmail.com***
[4] *Assistant Professor, Department of ECE, ALIET, AP, INDIA,* ***pbosebabu@gmail.com***

Abstract

Reversible logic has emerged as one of the most important approaches for the power optimization with its application in low power VLSI design. They are also the fundamental requirement for the emerging field of the Quantum computing having with applications in the domains like Nano-technology, Digital signal processing, Cryptography, Communications. Implementing the reversible logic has the advantages of reducing gate counts, garbage outputs as well as constant inputs. In contrast to conventional gates, reversible logic gates have the same number of inputs and outputs, each of their output function is equal to 1 for exactly half its input assignments and their fan-out is always equal to 1. It is interesting to compare both reversible and conventional gates. In this paper addition, subtraction, operations are realized using reversible logic gates like DKG and TSG gate and compared with conventional gates.

Index Terms: *Reversible logic, Quantum computing, Garbage outputs, Constant inputs*

----------***----------

1. INTRODUCTION

In order to discuss new trends and projects in the area of reversible logic one must first have an understanding of what this is. First of all, we'll restrict our discussion of logic functions to two-valued functions describing switching logic. Energy loss is an important consideration in digital circuit design, also known as circuit synthesis. Higher levels of integration and the use of new fabrication processes have dramatically reduced the heat loss over the last decades. The other part of the problem arises from Landauer's principle for which there is no solution. Landauer's principle states that logic computations that are not reversible necessarily generate kT * log 2 Joules of heat energy for every bit of information that is lost, where k is Boltzmann's constant and T the absolute temperature at which computation is performed. For room temperature T the amount of dissipating heat is small at (i.e. 2.9 $*10^{-21}$ Joules), but not negligible. This amount may not seem to be significant, but it will become relevant in the future. Consider heat dissipation due to the information loss in modern computers. First of all, current processors dissipate 500 times this amount of heat every time a bit of information is lost. Second, assuming that every transistor out of more than 4 * 107 for Pentium-4 technology dissipates heat at a rate of the processor frequency, for instance 2 GHz, the figure becomes 4*1019 * kT ln 2 J/sec. The processor's working temperature is greater than 400 degrees Kelvin, which brings us to 24 * 1021kT ln 2. A reversible logic circuit should have the following features:

· Use minimum number of reversible gates.
· Use minimum number of garbage outputs.
· Use minimum constant inputs.

2. REVERSIBLE GATES

The simplest Reversible gate is NOT gate and is a 1*1 gate. Controlled NOT (CNOT) gate is an example for a 2*2 gate. There are many 3*3 Reversible gates such as F, TG, PG and TR gate. The Quantum Cost of 1*1 Reversible gates is zero, and Quantum Cost of 2*2 Reversible gates is one. Any Reversible gate is realized by using 1*1 NOT gates and 2*2 Reversible gates, such as V, V+ and FG gate which is also known as CNOT gate. The V and V+ Quantum gates have the property given in the Equations 1, 2 and 3.

V * V = NOT …… (1)
V * V+ = V+ * V = I …….. (2)
V+ * V+ = NOT …… (3)

The Quantum Cost of a Reversible gate is calculated by counting the number of V, V+ and CNOT gates.

2.1 NOT Gate

The Reversible 1*1 gate is NOT Gate with zero Quantum Cost is as shown in the Figure 1.

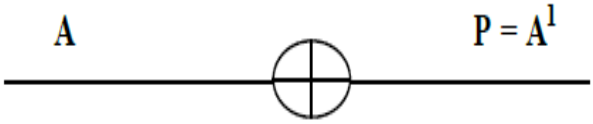

Fig1: NOT gate

2.2 Feynman / CNOT Gate

The Reversible 2*2 gate with Quantum Cost of one having mapping input (A, B) to output (P = A, Q = A B) is as shown in the Figure 2.

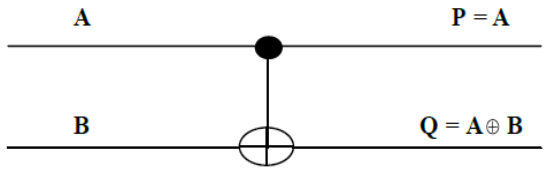

Fig 2: Feynman/CNOT gate

2.3 Toffoli Gate

The 3*3 Reversible gate with three inputs and three outputs. The inputs (A, B, C) mapped to the outputs (P=A, Q=B, R=A.B C) is as shown in the Figure 3.

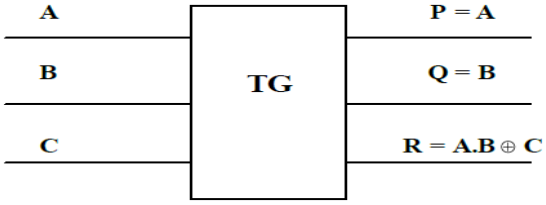

Fig 3: Toffoli gate

Toffoli gate [4] is one of the most popular Reversible gates and has Quantum Cost of 5. It requires 2V, 1V+ and 2 CNOT gates. Its Quantum implementation is as shown in Figure 4

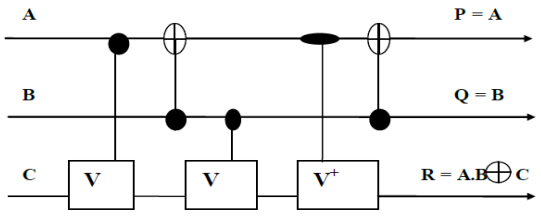

Fig 4: Quantum implementation of Toffoli gate

2.4 Peres Gate

The three inputs and three outputs i.e., 3*3 reversible gate having inputs (A, B, C) mapping to outputs (P = A, Q = A B, R = (A.B) C). Since it requires 2 V+, 1 V and 1 CNOT gate, it has the Quantum cost of 4. The Peres gate and its Quantum implementation are as shown in the Figure 5 and 6 respectivel

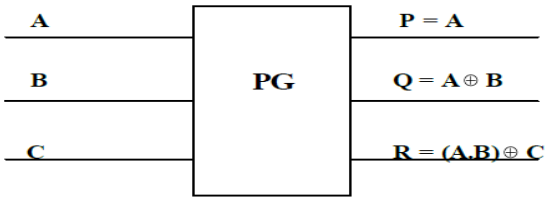

Fig5: Peres gate

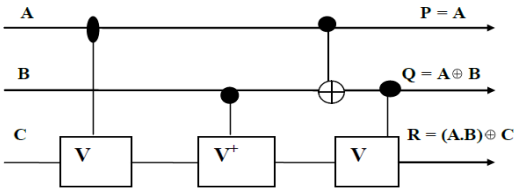

Fig6. Quantum implementation of Peres gate

2.5 Fredkin Gate

Reversible 3*3 gate maps inputs (A, B, C) to outputs (P=A, Q=A'B+AC, R=AB+A'C) having Quantum cost of 5 and it requires two dotted rectangles, is equivalent to a 2*2 Feynman gate with Quantum cost of each dotted rectangle is 1, 1 V and 2 CNOT gates. Fredkin gate and its Quantum implementations are shown in Figure 7 and 8 respectively.

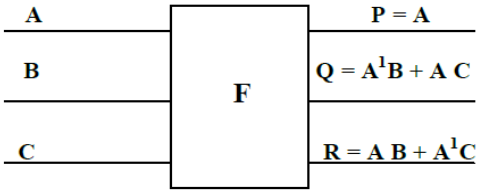

Fig7. Fredkin gate

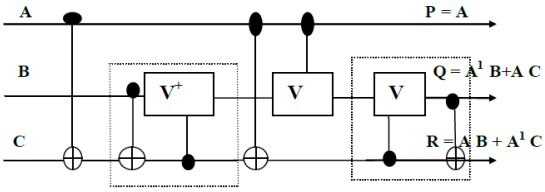

Fig8. Quantum implementation of Fredkin gate

3. REVERSIBLE DKG AND TSG GATE

A 4* 4 reversible DKG and TSG gates [6] can work singly as a reversible Full adder and a reversible Full subtractor is shown in Fig 9a. It can be verified that input pattern corresponding to a particular output pattern can be uniquely determined. Its implementation as a full adder and as a full subtractor is shown

in Fig 9b and 9c respectively. If input A=0, the proposed gate works as a reversible Full adder, and if input A=1, then it works as a reversible Full subtractor. It has been proved that a reversible full-adder circuit requires at least two garbage outputs to make the output combinations unique, which is the primary condition for a reversible circuit [5]. The proposed reversible full adder/subtractor circuit produces two garbage outputs, so it is optimal in terms of number of garbage outputs.

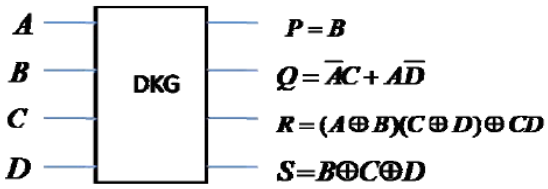

Fig 9: Reversible DKG gate [6]

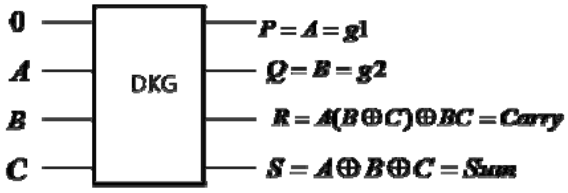

Fig 10: DKG gate implemented as Full adder [6]

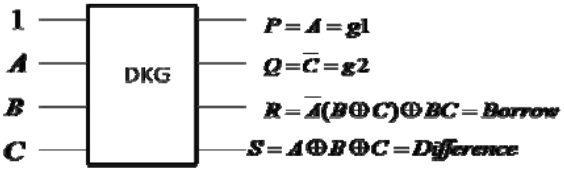

Fig11: DKG gate implemented as Full subtractor [6]

The binary Full adder/subtractor is capable of handling one bit of each input along with a carry in/borrow in generated as a carry out/ borrow from addition of previous lower order bit position. If two binary numbers each consisting of n bits are to be added or subtracted, then n binary full adders/subtractors are to be cascaded. A Parallel adder/subtractor is an interconnection of full adders/subtractors and inputs are simultaneously applied. The carry/borrow generated at a stage is propagated to the next stage. Thus, delay is more in such type of adders/subtractors. A 4 bit reversible parallel adder/subtractor is implemented using the reversible DKG gate and shown in Fig 10a. When the control input A=0, the circuit acts as a parallel adder, produces a 4 bit sum and a carry out, as shown in Fig 10b. If the control input A=1, the circuit acts as a parallel subtractor, produces a 4 bit difference and borrow out, as shown in Fig 10c. The same design can be extended to n bits.

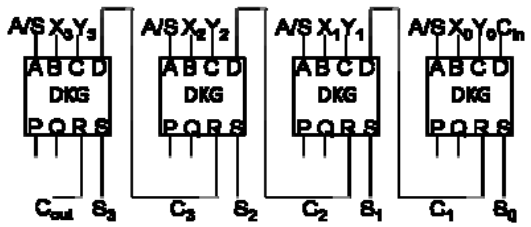

Fig 12: Reversible Parallel adder/Subtractor

The same ripple carry adder model is applied to the TSG reversible gate also, where it is having a change in the primary inputs and garbage outputs.

4. COMPARISION AND RESULTS

The comparison is carried out in between the reversible and conventional logic gates by using XILINX 9.1and program is written in VHDL language. . In reversible logic we use DKG and TSG gates for both adder/subtractor as it has low power consumption and less garbage output as already discussed in the section3. The comparison is carried out for the four operand four bit adder/subtractor in reversible and conventional gates.

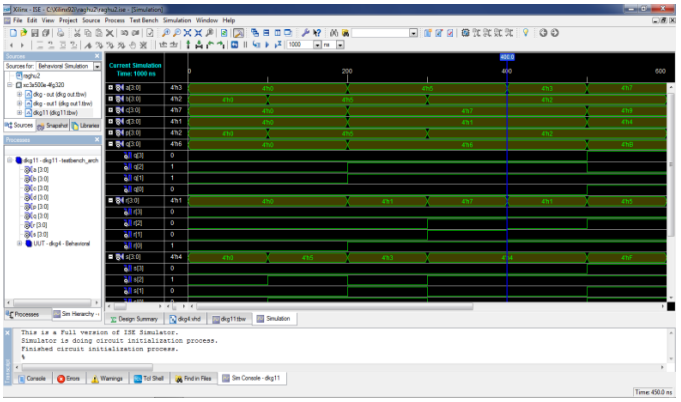

Fig13. Four bit DKG Adder.

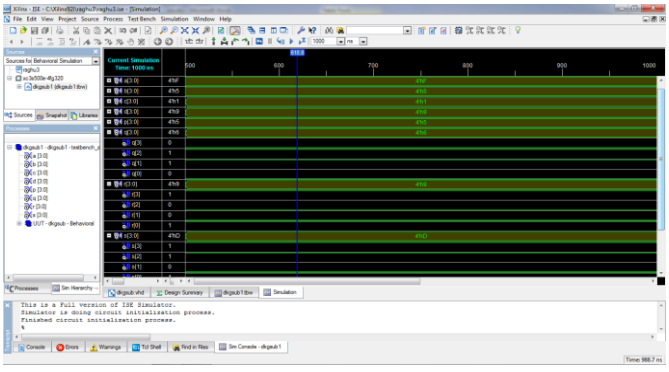

Fig14. Four bit DKG subtractor.

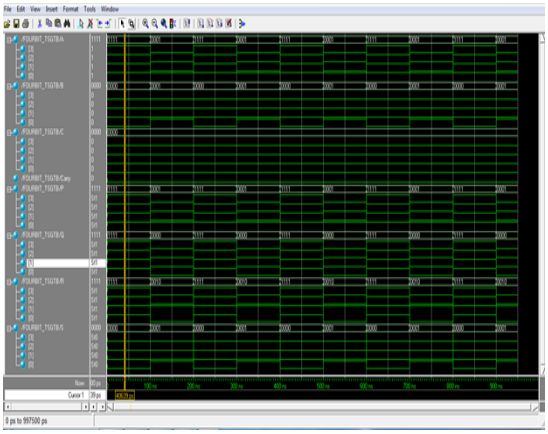

Fig 15. Four bit TSG adder.

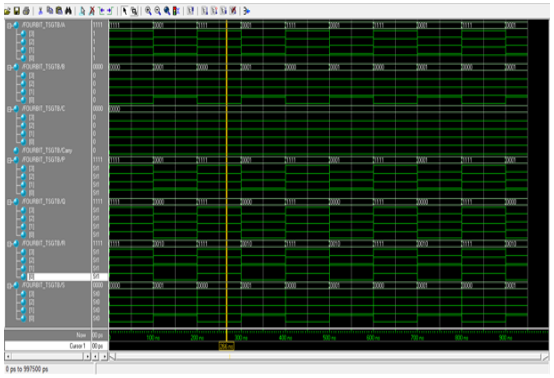

Fig16. Four bit TSG subtractor.

Table1. Comparison of power consumption and delay for reversible and conventional logic gates adder.

Para-meter	Basic gate adder four bit	Basic gate subtractor Four bit	Reversible DKG adder Four bit	Reversible TSG Adder Four bit
Power (w)	0.081073	0.08173	0.08143	0.08143
Delay (ns)	9.882	9.882	7.850	7.715

Table2. Comparison of 4bit subtractor for reversible and conventional gates.

Para-meter	Basic gate subtractor four bit	Reversible 4bit DKG Subtractor	Reversible 4bit TSG Subtractor
Power(mw)	81	0.08143(w)	0.6916
Delay(ns)	6.236	7.850	5.847
Area	16%	18%	23%
LUT`s	2	12	Don`t know

CONCLUSIONS

In this paper, we compared 4-bit reversible adder/subtractor circuit using DKG and TSG gates. Tables 1 and 2 demonstrates that the comparison is carried out for reversible adder/subtractor circuit is better than the existing designs in terms of hardware complexity, number of gates, garbage outputs and constant inputs. Furthermore, the restrictions of reversible circuits were highly avoided. Our proposed reversible adder/subtractor circuit can be applied to the design of complex systems in nanotechnology. All the proposed circuits are technology independent since quantum logic and Optical logic implementations are not available.

REFERENCES

[1]. C.H.Bennet,"logically reversibility of computation", IBM journal of research and development pp 525-532, NOV 1973.
[2]. R. Landauer,"Irreversibility and heat generation in the computation process" ,IBM journal of research and development, pp 183-191.
[3]. "A new reversible TSG gate and its application for designing efficient adder circuit" by Himanshu Thapliyal and M.B.Srinivas.
[4]."Design of low power arithmetic unit based on reversible logic" in International Journal of VLSI and signal processing applications, ISSN 2231-3133.
[5]."Optimal design of a reversible full adder" in International Journal of unconventional computing by Yvan Van Rentergen and Alexis De Vos.
[6]."A novel design of reversible serial and parallel adder/subtractor" in International journal of engineering science and technology by Krishnaveni.D and Geetha priya.M.
[7]."An improved design of a multiplier using reversible logic gates" in IJEST by Bhagya Lakshmi and Venkatesa.
[8]. Feynman R., 1985. Quantum mechanical computers, Optics News, 11: 11-20.
[9]. Low power reversible parallel binary adder/subtractor by Rangaraju H.G, Venugopal U, Muralidhara K.N, Raja K.B.